FABRICATION AND CHARACTERIZATION OF Au/n-Si SCHOTTKY BARRIER DIODES

A thesis submitted
in partial fulfilment of the requirements

for the degree of
Master of Technology

by
Md Tayyab Ansari

to the

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August, 1996

DEDICATED

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CERTIFICATE

This is to certify that the work contained in the thesis entitled "**Fabrication and characterization of Au/n-Si Schottky Barrier diodes**", by **Md. Tayyab Ansari**, has been carried out under my supervision and has not been submitted elsewhere for a degree.

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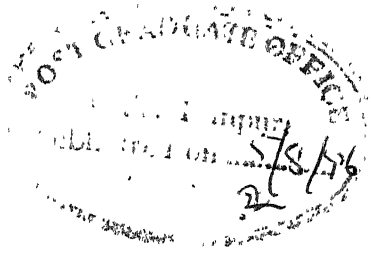

ABSTRACT

Au/n-Si Schottky barrier diodes have been fabricated by depositing a gold film of ≈ 600 $\mathring{A}$ thickness, using a thermal evaporation technique in vacuum $\approx 10^{-6}$ torr, on to a cleaned n-type silicon wafer of (111) orientation Their current-voltage (I-V) characteristics have been measured at room temperature and analysed on the basis of thermionic emission-diffusion (TED) mechanism, using a computer program The parameters, namely barrier height, ideality factor and series resistance are shown to vary from diode to diode, the reasonable values being $\phi_b \approx 0.79$ V, $\eta \approx 1.17$ and $R_s \approx 200 - 300$ Ω.

The values of barrier height obtained from the Capacitance-Voltage (C-V) characteristics are invariably higher than those derived from the (I-V) data. This discrepancy and high values of ideality factor are attributed to the prevailing barrier inhomogeneities at the gold-silicon interface. Based on X-ray diffraction, scanning electron micrographs and Rutherford back scattering spectrum, it is shown that gold does not react with silicon and thus form a pure metal-semiconductor junction. Further annealing of the diodes at 450°C for 30 minutes leads to the formation of gold globules and deterioration in their characteristics.

I-V characteristics of a Schottky diode have also been simulated using a TED current expression and assuming a Gaussian distribution of barrier heights. Finally, it is shown that the decrease of barrier height, abnormal increase of ideality factor and non-linearity in the activation energy plot of the saturation current (usually observed in prac-

tice) can be explained by assuming the presence of barrier height inhomogeneities at the metal-semiconductor interface.

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Md Tayyab Ansari

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A_d	Diode Area
A^{**}	Richardson constant
I_s	Saturation Current
ϕ_b	Barrier Height
η	Ideality factor
η_{ap}	Apparent Ideality Factor
R_s	Series Resistance
E_c	Energy of bottom of conduction band
E_F	Fermi Energy
E_V	Energy of top of valance band
k	Boltzmann's constant
q	Magnitude of electronic charge
V	Applied bias(positive for forward bias)
$\overline{\phi_b}$	Mean value of barrier height
ϕ_m	Work function of metal
ϕ_s	Work function of semiconductor
ϕ_o	Neutral level for surface states
χ_s	Electron affinity of semiconductor
T	Temperature in Kelvin
ϵ	Permittivity of semiconductor

σ Standard deviation

$\gamma = \frac{\partial \phi}{\partial V}$ (Positive derivative)

$\xi = \frac{\partial \sigma}{\partial V}$ (Positive derivative)

Chapter 1

Introduction

A rectifying metal-semiconductor (M-S) contact is known as a Schottky barrier diode and it exhibits asymmetrical electrical characteristics [1-2]. During the last century these contacts have experienced three major periods of industrial importance: first as radio detectors in early 1900s, then as radar detectors during the second world war and later on as clamping diodes, microwave diodes and gates of microwave transistors [3-5]. The first M-S device was the point contact diode made by pressing a metal whisker to a semiconductor crystal piece. These days a high vacuum system is employed to fabricate reproducible planar metal-semiconductor interface with uniform contact potential and current distribution over the junction area.

1.1 Formation of Schottky barrier

When a metal comes in intimate contact with a semiconductor, a potential barrier is created by separation of charges at the M-S interface. Concurrently, a high resistance region devoid of mobile charges is formed within the semiconductor near the interface Schottky and Mott explained the mechanism of barrier formation on the basis of the difference in the work functions of the metal and the semiconductor. Fig.1.1a illustrates the energy band diagram of a case in which the metal has a larger work function compared to (say) the n-type semiconductor. When the metal and n-type semiconductor are brought into contact,

electrons transfer take place from semiconductor to metal until Fermi levels get aligned and equilibrium is established. Electrons movement towards metal causes depletion in the semiconductor near the interface. Since the separation between the conduction band edge E_C and Fermi level E_F increases with decreasing electron concentration, the conduction band edge turns upwards near the interface. The migration of electrons leaves positively charged donors in the semiconductor and forms a thin sheet of negative charges at the metal surface. This produces an electric field in the direction opposite to electrons flow, i.e., from the semiconductor to the metal The width of the space charge layer in the semiconductor is appreciable because donor density being several orders of magnitude smaller than the electron concentration in the metal. Since the band gap of the semiconductor remains unchanged after the contact, the valence band edge E_V also moves upwards identically to the conduction band edge E_C. Further, the vacuum level in the semiconductor follows a similar trend and bends exactly as E_C. Thus, for a M-S system in thermal equilibrilium the vacuum level remains continuous across the transition region. The amount of band bending is then just equal to the difference between the two vacuum levels (see, e g., Fig.1 1b). Thus,

$$qV_i = \phi_m - \phi_s \tag{1.1}$$

where V_i is the built in potential at the junction, ϕ_m and ϕ_s are the work functions (in units of eV) of metal and semiconductor, respectively. The V_i represents the potential barrier which an electron has to overcome while moving from the semiconductor to the metal. The corresponding energy is qV_i. The barrier (ϕ_b) as seen from the metal side is given by $\phi_b = \phi_m - \chi_s$ or $= \phi_m - (\phi_s - \phi_n)$, since $\phi_s = \chi_s + \phi_n$.Using eq. (1.1), we have

$$\phi_b = qV_i + \phi_n \tag{1 2}$$

where χ_s is the electron affinity and $\phi_n = E_C - E_F$ represents the penetration of the Fermi level in the band gap of the semiconductor. Obviously, $\phi_b > qV_i$. The exact shape of the barrier is determined from the charge (or donor) distribution within the space charge layer. Schottky assumed the semiconductor to be uniformly doped, giving a constant charge density in the depletion region. The electric field strength therefore rises linearly with distance from the edge of the space charge layer. Mott assumed a thin layer devoid of charges sandwiched between a uniformly doped semiconductor and the metal. The electric field strength within the so called depletion region is constant. Fig.1.1 bshows the thermal

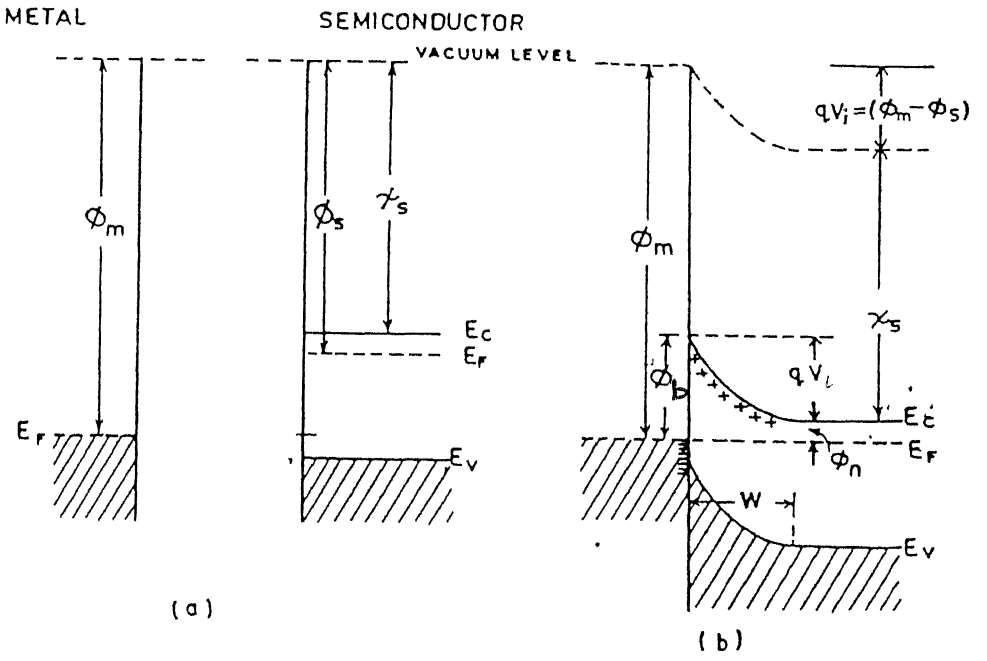

Fig. 1.1 Electron energy band diagrams of metal and n-type semiconductor having $\phi_m > \phi_s$ (a) neutral metal and semiconductor separated from each other, (b) after the contact and attaining thermal equilibrium .

equilibrium energy band diagram of the M-S contact The depletion region of width w has few mobile carries and therefore displays very high resistance. Consequently, a large part of the externally applied voltage drops across the depletion region. If a negative voltage (V_F) is applied at the semiconductor, the depletion region width decreases and voltage across it falls from V_i to (V_i - V_F). The electrons now see a reduced barrier and move from the semiconductor towards the metal causing a current flow. Since no voltage drop occurs within the metal, ϕ_b remains unaffected and there is no electron flow from metal to semiconductor. Thus,M-S junction exhibits rectifying properties

1.2 The concept of surface states

As per eq.(1.1), the barrier height should increase linearly with ϕ_m, but, is found to be not so in practice. The discrepancy has been explained by Bardeen [6] on the basis of suface states. Accordingly, broken covalent (or dangling) bonds at the semiconductor surface give rise to localized energy states, called surface states. These are believed to be distributed in the band gap and characterized by a neutral level ϕ_o. That means when there is no band bending in the semiconductor, the surface states are occupied right up to ϕ_o making the surface neutral, i.e., a flat band condition shown in Fig.1.2a. The states below ϕ_o are donor like and those above ϕ_o behave like acceptors. Their presence leads to the redistribution of the charge near the semiconductor surface and affect the barrier height. The equilibrium is established when sufficient number of electrons from the semiconductor adjacent to the surface occupy the localized states lying above ϕ_o. The surface then becomes negatively charged and a depletion layer consisting of ionized donors is created near the semiconductor surface. Thus, a potential is formed even in the absence of the metal contact as depicted in Fig 1.2b. If a metal is now brought into contact with the semiconductor and equilibrium reached, the Fermi level in the semiconductor changes by an amount equal to the contact potential difference through transfer of electrons to the metal. If the density of surface states is high, the charge exchange takes place largely between the metal and the surface states and the space charge in the semiconductor nearly remains unchanged. As a result, barrier height becomes independent of the metal work function and is given by [6]

$$\phi_b = (E_g - \phi_o) \tag{1.3}$$

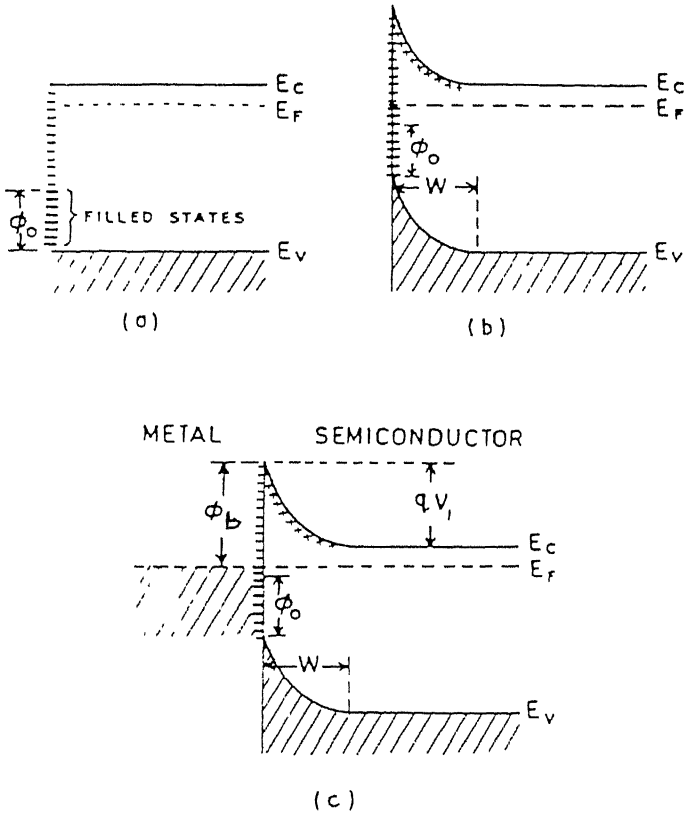

Fig. 1.2 Electron energy band diagrams of n-type semiconductor with surface (a) under flat band , (b) in thermal equilibrium with the bulk , and (c) in contact with a metal.

In this case, the barrier height is said to be "pinned" by surface states. Eq. (1.3) is known as the Bardeen limit.

1.3 Conduction mechanisms

The current flows across a Schottky barrier diode because of charge transport from the semiconductor to the metal or vice-versa through several different mechanisms namely, thermionic emission-diffusion, tunneling, generation or recombination, and minoriy carrier injection. In addition, there may be leakage current due to high electric field at the contact periphery or interface current due to traps at the metal-semiconductor interface.

1.3.1 Thermionic emission-diffusion mechanism

It is the dominant transport mechanism in the Schottky barrier diodes and involves drift and diffusion both [7]. The electrons in the conduction band are assumed to have kinetic energy only and barrier height ϕ_b is much larger than (kT/q). The net current due to flow of electrons from semiconductor to metal by overcoming the potential barrier of height ϕ_b at a forward bias V is given by [8,9]

$$I = A_d A^{**} T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp(\frac{qV}{kT}) - 1\right] \qquad (1\ 4)$$

Where A^{**} is the effective Richardson constant, A_d is the diode area, T is the temperature in kelvin, k is the Boltzmann constant, q is the electronic charge and h is the Planck's constant For free electrons, the Richardson constant A^{**} is $1.12 \times 10^6\ m^{-2}K^{-2}$. In deriving eq.(1.4) diffusion of carries is also included. However, the barrier height invariably increases with the forward bias. If the barrier height is assumed to vary linearly with bias, we have

$$\phi_b(V) = \phi_{bo} + \gamma V \qquad (1.5)$$

Where ϕ_{bo} is the barrier height at zero bias and $\gamma(= \partial\phi_b/\partial V)$ is positive. Substituting the value of $\phi_b(V)$ into eq.(1.4) yields

$$I = I_s exp\left(\frac{qV}{\eta kT}\right)\left[1 - \exp(\frac{-qV}{kT})\right] \qquad (1.6)$$

where

$$I_s = A_d A^{**} T^2 \exp\left(\frac{-q\phi_{b0}}{kT}\right) \tag{1.7}$$

and $1/\eta = 1 - \gamma$. The parameter η is called the ideality factor and usually has a value greater than unity. The neutral region of the semiconductor offers resistance (R_s) and so significant voltage drop occurs there at large forward currents. As a consequence, voltage across the Schottky barrier region is reduced by a factor IR_s and resulting current becomes

$$I = I_s \exp\left(\frac{q(V - IR_s)}{\eta kT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \tag{1.8}$$

Now a plot of ln(I) vs V deviates from a straight line and exhibits saturation at high forward voltages.

1.3.2 Tunneling through the barrier

This mechanism prevails when the semiconductor is heavily doped such that the Fermi level lies above the bottom of the conduction band and the depletion region width is very small. Consequently, at low temperatures, electrons having energy nearly equal to the Fermi level can tunnel from the semiconductor into the metal. The tunneling current through the barrier is of the form [9]

$$I_t = I_{to} \exp(\frac{qV}{E_o})[1 - exp(\frac{-qV}{kT})] \tag{1.9}$$

where

$$E_o = E_{oo} \coth(\frac{E_{oo}}{kT}) \tag{1.10}$$

and I_{to} is the tunneling saturation current The parameter E_{oo} is defined as

$$E_{oo} = \frac{h}{4\pi}\sqrt{\frac{N_d}{m_e^* \epsilon_s}} = 18.5 \times 10^{-15}\sqrt{\frac{N_D}{m_r \epsilon_r}} \qquad eV \tag{1.11}$$

where $m_e^* (= m_r m_o)$ is the effective mass of electron and $\epsilon_s (= \epsilon_r \epsilon_o)$ is the permittivity of the semiconductor, m_o is the electron rest mass and N_D is the donor concentration in m^{-3}. The process is called field emission (FE) when $E_{oo} >> kT$. At high temperatures where $E_{oo} \approx kT$, the tunneling of thermally excited electrons occurs and the process is called

thermionic-field emission (TFE). It may be noted that TFE also causes a reduction in the barrier height by [9]

$$\Delta\phi = \left(\frac{3}{2}\right)^{\frac{2}{3}} E_{oo}^{\frac{2}{3}} V_d^{\frac{1}{3}} \tag{1.12}$$

Where V_d stands for the voltage corresponding to the band bending. Eq.(1.9) suggests that the $lnI_t/[1 - exp(\frac{-qV}{kT})]$ versus V plot should yield a straight line with slope giving E_o and the intercept at zero bias the saturation current I_{to}.

1.3.3 Carrier generation and recombination

At zero bias, the rate of electron-hole pair generation in the depletion region is balanced by the rate of recombination and therefore there exists a thermal equilibrium. The electron-hole product (np) is then equal to n_i^2. However, with the application of the bias, np product departs from n_i^2 and a net generation or recombination of carriers occur depending upon the polarity. In case of a Schottky diode made on n-type silicon, substrate is forward biased the electrons are injected into the depletion region from the neutral bulk semiconductor and holes swept away from the metal. These additional electron-hole pairs combine in the depletion region to give a forward combination current. Such a process occurs most effectively through recombination centres (or traps) with energy levels lying near the centre of the band gap. The recombination current can then be described by [9]

$$I_r = I_{ro}[exp(\frac{qV}{2kT}) - 1] \tag{1.13}$$

with

$$I_{ro} = \frac{qn_i A_d w}{2\tau} \tag{1.14}$$

and

$$n_i = \sqrt{N_C N_V} exp\left(\frac{-E_g}{2kT}\right) \tag{1.15}$$

Here w is the width of the depletion region, τ is the carrier effective life time within the depletion region, n_i is the intrinsic carrier concentration, E_g is the energy band gap, and N_C and N_V are the effective conduction and valence-band density of states, respectively. When the Schottky diode is reverse biased additional electron-hole pairs are generated in the depletion region and cause a generation current in the reverse direction.

1.3.4 Minority carrier injection

The Schottky barrier diode is a majority-carrier device under the low bias conditions. However, at large forward bias, minority carrier current contribution increases and become more than the diffusion current. For example when the barrier height of the semiconductor (say n-type) is more than half of its band gap the interface region adjacent to the metal becomes essentially p-type. Under a forward bias, the electrons from the semiconductor flow into the metal and some of the holes are swept into the neutral region. Thus, injection of holes occur from the metal into the semiconductor. It may be noted that the process is equivalent to flow of electrons from the semiconductor valence band into the metal directly. The current I_p caused by hole injection from metal into the neutral region of n-type semiconductor of donor concentration N_D is given by [10]

$$I_p = \frac{qA_d D_p n_i^2}{N_D L_p}\left[exp(\frac{qV}{kT}) - 1\right] \tag{1.16}$$

Where D_p is the hole diffusion constant and $L_p = \sqrt{D_p \tau_p}$ is the hole diffusion length. τ_p represents the hole lifetime in the neutral region and other terms have their usual meanings. Thus, the ratio of hole current I_p and the thermionic emission-diffusion current I, given by eq.(1 4), is written as

$$\frac{I_p}{I} = \frac{qN_C N_V}{A^{**} N_D T^2}\sqrt{D_p \tau_p} exp\left(\frac{q\phi_b - E_g}{kT}\right) \tag{1.17}$$

Here, we have made the substitutions $L_p = \sqrt{D_p \tau_p}$ and n_i from eq.(1.15). Thus, the ratio (I_p/I) increases with the increase of barrier height (ϕ_b) and diffusion constant D_p and decrease of N_D, τ_p and T. Yu and Snow [10] have shown that (I_p/I) is less than 0.1 for Schottky barriers on n-type silicon having $\phi_b = 0.8$ V and $N_D >> 10^{20} m^{-3}$. At still large forward bias, significant voltage drop occurs within the neutral region of the semiconductor and causes a drift current as well and total minority carrier current increases substantially. The critical current I_c beyond which the (I_p/I) increases almost linearly is given by [11]

$$I_c = \frac{qD_n A_d N_D}{L} \tag{1.18}$$

Where L is the width of quasi neutral region of the n-type semiconductor and D_n is the electron diffusion constant.

1.4 Methods of barrier height measurement

The current through a Schottky barrier diode at a forward bias V, based on the thermionic emission-diffusion mechanism is given by the eq.(1.8). For the forward bias V in excess of 3kT/q, the plot of ln(I) vs V is linear upto a point (IR_s) term remains ineffective but deviates afterwards and shows saturation. The straight line portion of ln(I) vs V plot extrapolated to zero bias yields $\ln(I_s)$ as intercept at the ordinate. Substituting the values of I_s and the effective Richardson constant A^{**} in eq.(1.7), zero-bias barrier height ϕ_{bo} can be determined for a given diode area A_d at any temperature T. It may be mentioned that the value of ϕ_{bo} is not very sensitive to the choice of A^{**}, since at room temperature a 100% increase in A^{**} causes a increase of only 0.018 V in ϕ_{bo}. Alternatively, one can make $\ln(I_s/T^2)$ vs 1/T plot (termed as activation energy or Arrhenius plot) by finding out saturation current at various temperatures and obtain the value of ϕ_{bo} from the slope of the best fit straight line itself. Also, the intercept at the ordinate gives $ln(A^{**}A_d)$, the product of the electrically active area A_d and the effective Richardson constant A^{**}. The principle advantage of this approach is that value of electically active area A_d is not at all required for the evaluation of ϕ_{bo}.

The barrier height can also be determined by measuring the capacitance of the Schottky diode as a function of reverse d.c. bias (V_R) When a small a.c voltage of a few mV is superimposed upon a d.c. bias, charges of opposite signs are induced on the metal surface and in the depletion region of the semiconductor. The relationship between the capacitance (C) and reverse bias V_R is given by [1]

$$C = A_d \sqrt{\frac{\epsilon_s q N_D}{2(\phi_b - \phi_n - V_R - \frac{kT}{q})}} \tag{1.19}$$

where ϵ_s is the permittivity of the semiconductor, N_D is the dopant concentration, ϕ_n is the distance of the Fermi level from bottom of the conduction band and other symbols have their usual meaning. Thus, a plot of $1/C^2$ versus V_R gives a straight line with slope of $(2/{A_d}^2 \epsilon_s q N_D)$ and an intercept on the voltage axis V_{RO} at which $1/C^2$ is zero. The value of barrier height ϕ_b can then be obtained easily as

$$\phi_b = V_{RO} + \phi_n + \frac{kT}{q} \tag{1.20}$$

and ϕ_n, the depth of Fermi level below the conduction band, can be computed from the doping concentration (N_D). Notice that N_D can be evaluated from the slope of $1/C^2$ vs V_R plot too.

1.5 Importance and applications

The most important commercial application of Schottky diodes is in bipolar integrated circuits as clamps and to a lesser extent as load resistor substitutes, diode couplers and level shifters. They are also used as discrete microwave transistors, optical and nuclear particle detectors, etc. All the practical applications, in fact, exploit the inherent high speed advantages of majority carrier conduction. Metal-semiconductor rectifiers are relatively immune to the speed limitation associated with the minority carrier storage in p-n junction devices [12-14]. The advantages of Schottky diode over p-n junction lies in its fast switching speed of about 1 ns, high forward conductance per unit area, large reverse impedance, compact size, structure which is easily integrated and fabrication at nearly low temperatures The disadvantages stems from the fact that the Schottky diode is a surface device and consequently sensitive to surface contamination and perimeter effects

1.6 Objective of the present work

Extensive studies have been undertaken on different aspects of Schottky barrier diodes with the view to understand their characteristics better and find newer applications [3,9,15-18].

The most important aspect of metal-semiconductor contacts is the process which determines the flow of charges over the barrier from the semiconductor to the metal and vice-versa. Detailed knowledge of the conduction process involved is needed to extract the values of the barrier parameters. The reports available in the literature provide information about the conduction mechanisms. But these vary in the interpretation of the I-V and C-V characteristics of a variety of Schottky diodes fabricated on n- and p- type silicon with different metals or silicides. Chand and Kumar [19,20] have studied I-V characteristics of Pd_2Si/silicon junctions over a wide temperature range and interpreted the results on the basis of thermionic emission-diffusion (TED) mechanism and assuming Gaussian distribution of barrier heights. Suzuki et al. [21] have studied C-V characteristics of $Al - SiO_2 - SiC$ at different frequencies under dark and illuminated conditions. The I-V characteristics of Schottky diodes formed by depositing various metals such as Ir, Pt, Cr, Er, W, Cu, Ti and Pd on silicon have been studied in detail [22-31]. However, a few brief reports are available on the gold based M-S junctions [32-37]. Horvath [32] has measured C-V

characteristics of Au/n-GaAs Schottky contacts and interpreted them on the basis of log normal lateral distribution of barrier heights. Sadiq and [illegible][33] have studied Au/p-AlSb Schottky contacts.

Chen et al. [34] have measured photovoltage, internal photo emission, and current-voltage (I-V) and capacitance-voltage (C-V) characteristics of Au/n-Si(111) Schottky barrier diodes in a temperature range of 7-300 K. Both the C-V and internal photo-emission data are found to yeild reliable values of barrier height and exhibit a negative temperature coefficient identical to that of the indirect band gap in silicon. On the other hand, photo voltage and I-V characteristics are shown to give lower values of barrier height due to the recombination current and display a strong positive temperature dependance. At room temperature, the barrier height obtained is 0.8V and idealty factor $\eta = 1.1$.

An attempt has been made here to fabricate Au/n-Si Schottky diodes and study their I-V and C-V characteristics. The advantage with gold is that it does not react with silicon and, therefore, can possibly lead to a true metal-semiconductor junction. In addition, simulation of I-V characteristics has been carried out on the basis of TED mechanism and assuming barrier inhomogeneities with a view to understand the effect of various barrier parameters in detail.

Chapter 2

Experimental Details And Procedures

2.1 Fabrication of Schottky diodes

The Au/n-Si Schottky barrier diodes were prepared on a n/n^+ silicon wafer of (111) orientation having a 8-9 $\mu\, m$ thick epitaxial n-layer of resistivity 0 9 $\Omega - cm$ over the underlying heavily doped n^+ region of resistivity 0.01 $\Omega - cm$. The overall thickness of the wafer was around 1 mm. For this, the wafers were first degreased with soap solution and then cleaned with organic solvents, namely trichloroethylene, acetone and methanol in succession in an ultrasonic cleaner and dried. Subsequently, wafer was etched in hydrofluoric acid for 1 min., rinsed in distilled water, and dipped in methanol until transferred to a vacuum chamber after drying with a hot air blower. The wafer was exposed to air for minimum possible time during this process. After attaining a vacuum $\approx 10^{-5}$ torr in the chamber, a thick film of aluminium was deposited by thermal evaporation method on the n^+ side of the wafer and annealed in a furnace after introducing into a quartz tube at 450°C for 30 min under vacuum $\approx 10^{-5}$ torr. Subsequently, wax was applied on aluminium deposited side and wafer treated with dilute HF (HF:H_2O = 1·10) for removal of the silicon dioxide layer (usually formed on silicon), cleaned in trichloroethylene, acetone and methanol in succes-

sion and submerged in methanol until introduced again in the vacuum chamber for gold deposition on the epitaxial n-layer The quantity of gold m (gm) for thermal evaporation was predetermined from [38] $m = 2\pi\rho tr^2$

where 2π is the solid angle in which evaporation occurs at the source (i.e tungsten boat), ρ is the density of gold (19 3 gm cm^{-3}), t is the required thickness (i e , 400$\mathring{A}$) of the film and r is the distance of the wafer from the boat. Gold charge was placed in a tungsten boat mounted in the work chamber. The wafer was also placed suitably at a predetermind distance away from the boat After attaining vacuum $\approx 10^{-5}$ torr as before, gold was deposited by passing a low voltage high amperage current through the tungsten boat on to the epitaxial n-layer (i.e., front side) of the silicon wafer through holes (1mm diameter) in the metal mask to form Schottky junctions. The wafer was later removed from the vacuum chamber and cut into small pieces to separate out the diodes. Each diode was then fixed on multipin header with silver paste keeping gold deposited portion upward. The circular gold portion of diodes were connected to header pins using very fine gold wires. Finally, one pin was connected to the body of the header by silver paste to get connection of the semiconductor side of the Schottky barrier diode.

2.2 I-V and C-V measurement

Fig 2.1 shows schematically the experimental set-up used for current-voltage (I-V) measurement of the Au/n-Si Schottky diodes. A programmable voltage source Keithley model 230 and an autoranging picoammeter Keithley model 485 were employed for bias application and measurement of the current, respectively. These were in fact interfaced with a personal computer Zenith PC-XT 286 for ensuring automatic recording of current at voltage step of 0.01V in the range 0.01-0.6 V. For achieving steady-state conditions, a delay of a few seconds was maintained in the subsequent measurement. Moreover, an average of three current readings were taken at each voltage step.The circuit diagram for the current-voltage measurement is shown in Fig 2.2 . The capacitance of Au/n-Si Schottky diode was measured using an impedance / gain-phase analyzer model HP4194A at a test frequency of 1 MHz under the reversed biased condition, i e., in the range of 0-4V with a step of 0.1V.

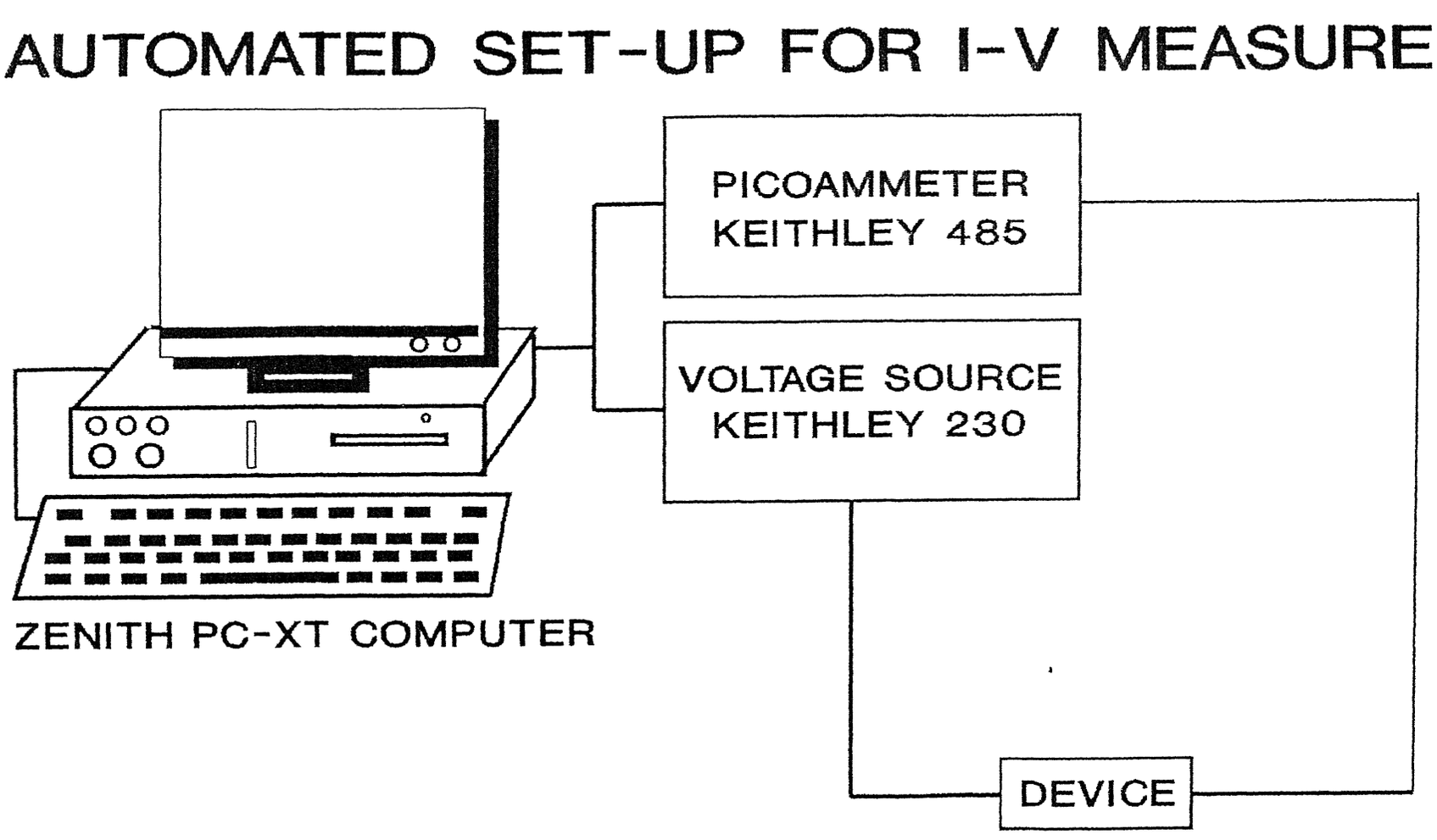

Fig. 2.1 Schematic diagram of the automated experimental set-up used for current-voltage (I-V) measurement .

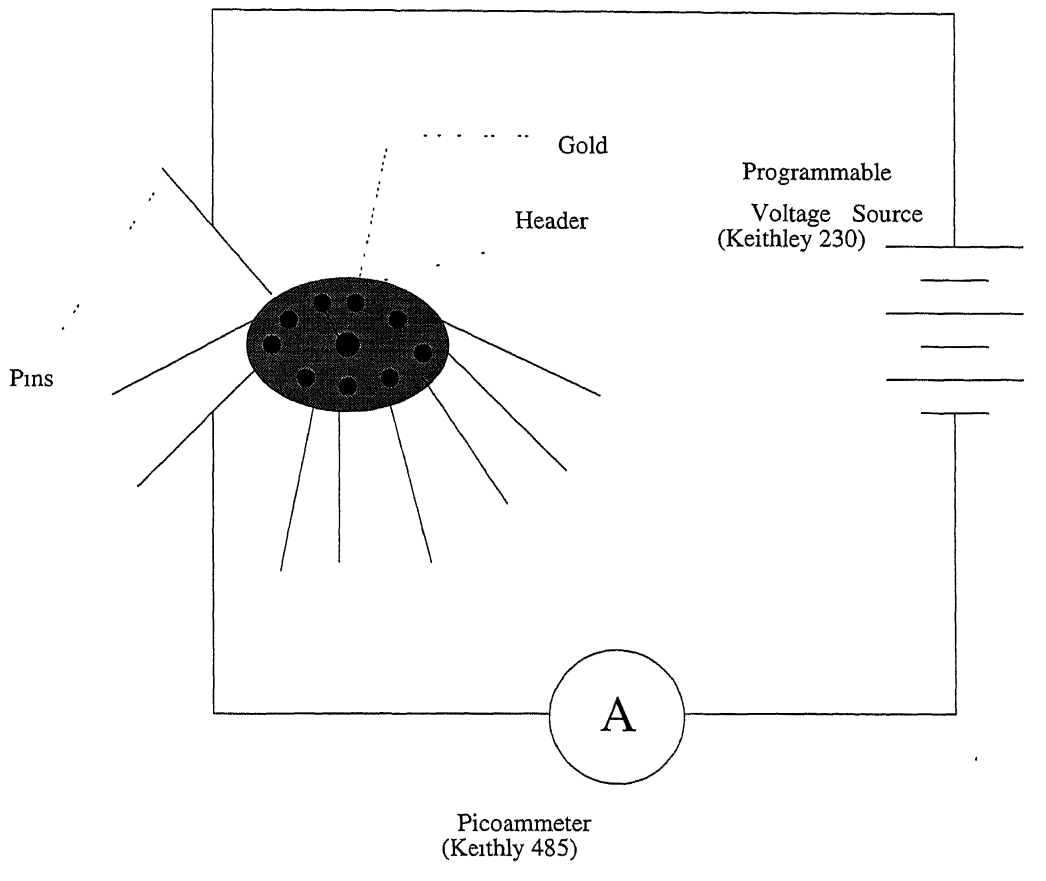

Fig 2.2 Circuit diagram of the current-voltage (I-V) measurement set-up .

2.3 Phase evaluation and microstructure

Another set of Schottky barrier diodes were fabricated in the same run or under identical experimental conditions but without using any mask to get large area coverage for phase evaluation through X-ray diffraction and microstructure examination under a scanning electron microscope. A Rich Seifert ISO-Debyeflex 2002 X-ray diffractometer with $Cu\ K\alpha$ radiation ($\lambda = 1.5418\mathring{A}$) was used for identification of phase(s) and changes resulting due to annealing of samples at 450°C for 30 min. The microstructure was analyzed using a scanning electron microscope model JEOL JSM 840A in the secondary electron (SE) mode.

2.4 Rutherford backscattering spectrometry (RBS)

The Rutherford backscattering spectometry set-up consists of
(a) a 2 MeV Van-de-Graaff accelerator for production and acceleration of Helium ions, (b) an electromagnet for dispersion of ions in terms of their mass and energy, (c) ion beam focussing unit, (d) separator for removal of oxygen from the $4He^+$ ions of the same energy, (e) a specimen backscattering chamber, and (f) detector assembly and analysis system was used. Fig 2.3 shows schematic digram of the backscattering chamber Sample holder plate (size 130 mm × 25 mm × 2.5 mm) is fixed from the top in such a way that the ion-beam entering from one of the port is incident normally to its surface. An aluminium grid is placed around the sample holder and applied a negative voltage of -180V to suppress the emission of secondary electrons, resulting due to ion beam irradiation, from the specimen surface. The ion beam current ≈5-10 nA was utilized. It was measured and integrated using a current integrator Ortec model 401 to obtain the total amount of charge. The scattered ions are allowed to fall on the detector placed at 30° from the normal to the specimen surface. The resulting signal is fed to a charge sensitive preamplifier Ortec model 142, a main amplifier Ortec model 572 and biased amplifier Ortec model 444 in succession to obtain output as voltage pulses. These voltage pulses are then collected in the multichannel analyzer (MCA) model - ND65 operating in the pulse height analyser (PHA) mode. The information is finally stored in a personal computer for display of the spectrum and further analysis, using suitable programs.

The Rutherford backscattering spectrum of Au/n-Si Schottky barriers were obtained

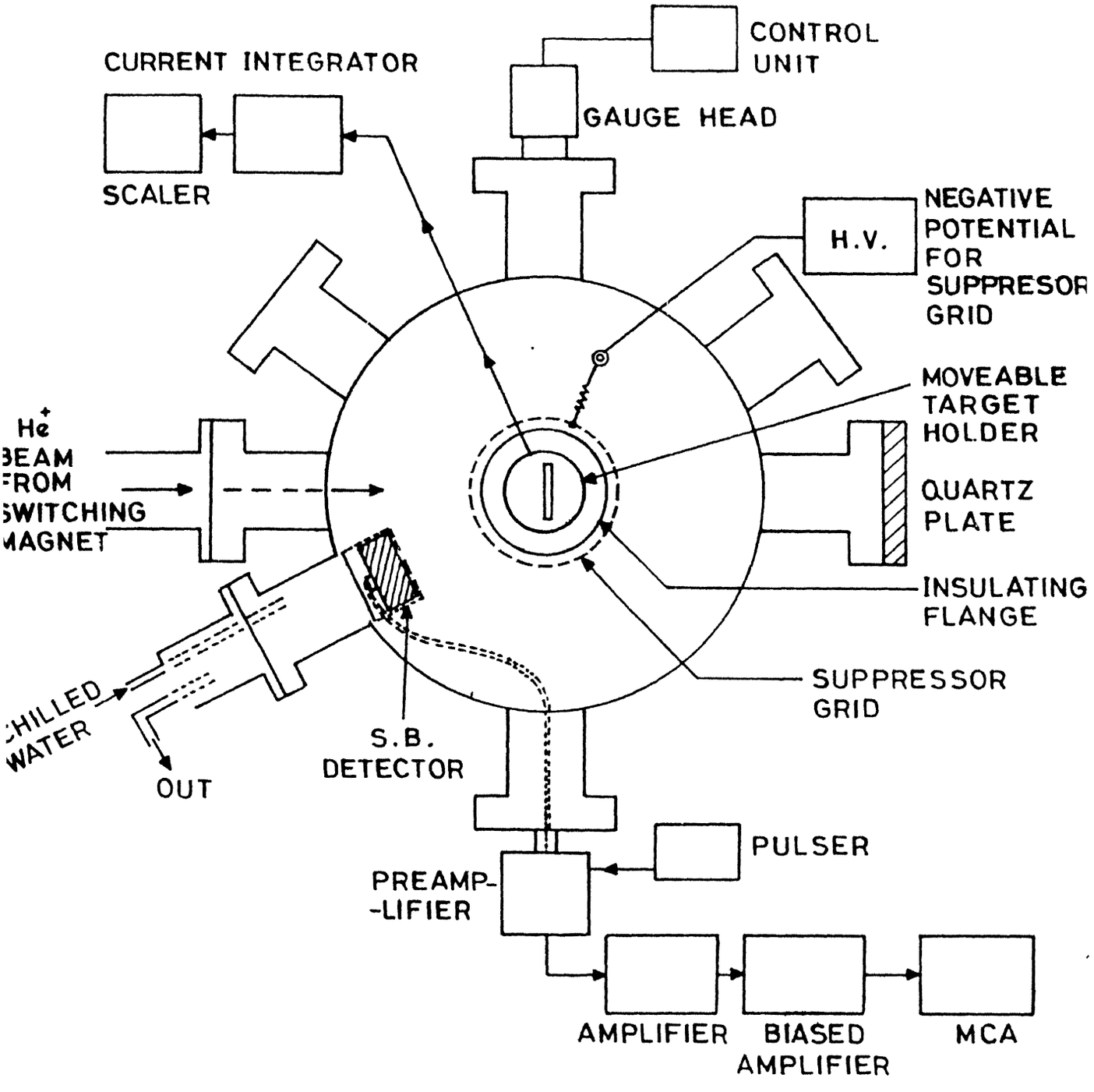

Fig. 2 .3 Schematic diagram of the Rutherford backscattering spectrometry (RBS) chamber

using $4He^{+}$ ions of 1.3 MeV at a scattering angle (θ) of 30°, the detector solid angle (Ω) of 2 57 milli-steridian and beam dose of 2μC It is customary to plot the normalized backscattering yield with respect to channel number/ ion energy. The normalized yield is given by Normalized Yield = (raw counts× corr) /($Q \times d\Omega \times \delta E$)

where raw counts represent the actual counts recorded, corr is the correction factor to compensate for inaccuracies during charge integration, Q is the beam dose in μC, $d\Omega$ is the solid angle in milli-steridian and δE is the calibration factor of the MCA in KeV/channel. The information about the depth distribution of the diffusing element in the sample and/or thickness of the deposited film can be obtained from the RBS spectrum[38].

Chapter 3

Results and discussion

3.1 Forward I-V characteristics

The forward current-voltage (I-V) characteristics of Au/n-Si (111) Schottky barrier diodes at 300 K are shown in Figs. 3.1 and 3.2. The plot is linear over several order of current, indicating thereby the dominance of thermionic emission- diffusion mechanism. At higher forward bias, ln(I) vs V plot deviates from the straight line because voltage drop across the series resistance (R_s) become effective. The fitting procedure involves iteration and takes I_s, η and R_s as adjustable parameters. A ln[I/(1-exp(-qV/kT))] versus V plot is usually made to include voltage regime $V < 3kT/q$ as well in the analysis. Needless to say that $[1-exp(-qV/kT)]$ factor assume significance at low bias and cause bending of the ln(I) vs V plot (see e.g., Fig.3.1). The linear portion on extrapolation gives the intercept at the ordinate as $\ln(I_s)$. Also, the slope of the associated straight line yields the ideality factor. However, the nature of the plot usually makes the straight line portion quite subjective and leads to uncertainties and error in the value of $\ln(I_s)$. So, a computer program in basic has been used to fit the experimental I-V data in thermionic emission - diffusion current eq.(1.8) [19]. The computer program is initially run by assuming the ideality factor η and series resistance R_s to be unity and zero, respectively, principally to obtain an approximate value of saturation current (I_s) and that fits the experimental data. This I_s is then introduced into eq.(1.8) and program is run again to determine the values of η and

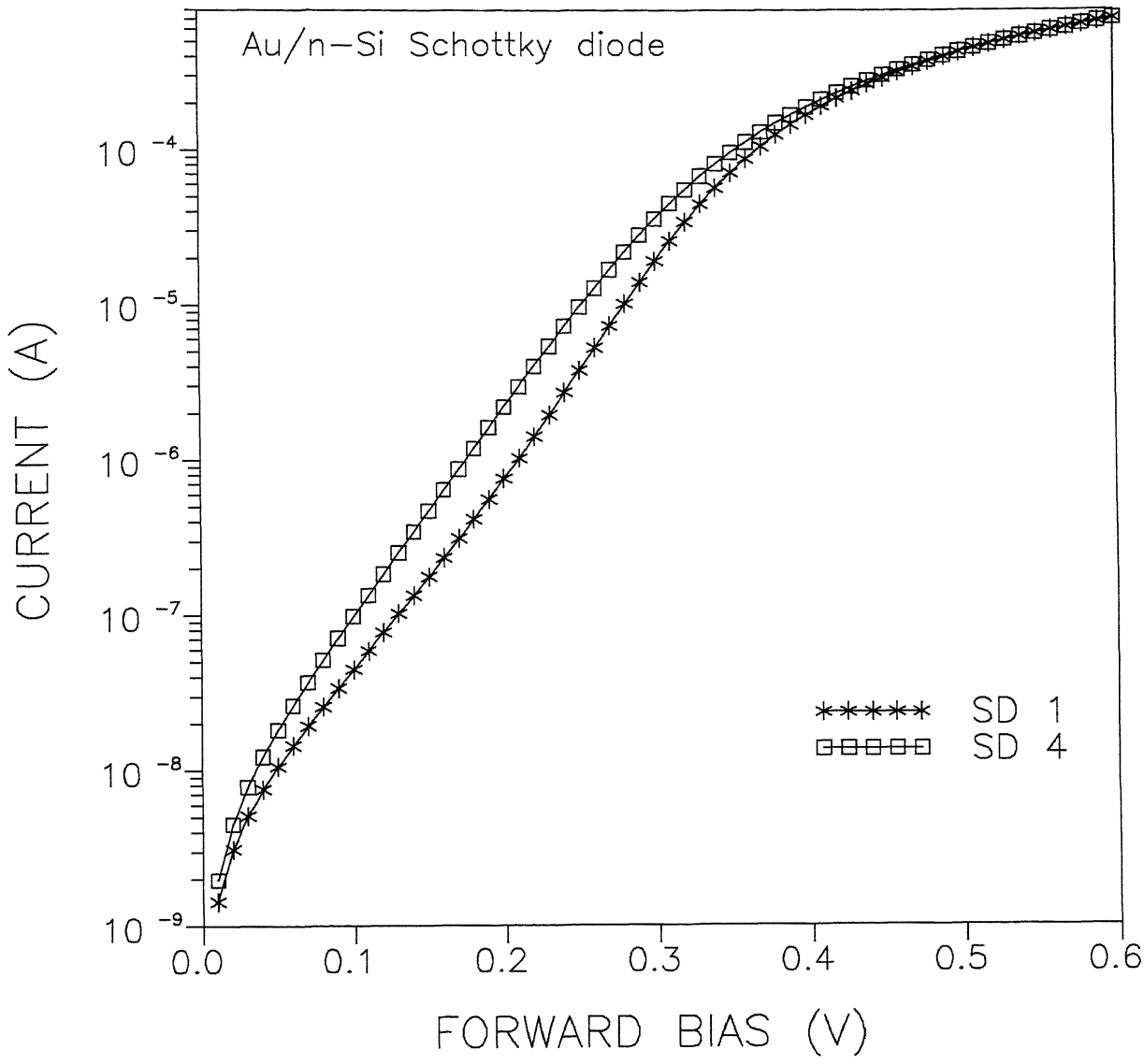

Fig 3.1 Forward Current-Voltage (I-V) characteristics of Au/n-Si Schottky barrier diodes at room temperature.

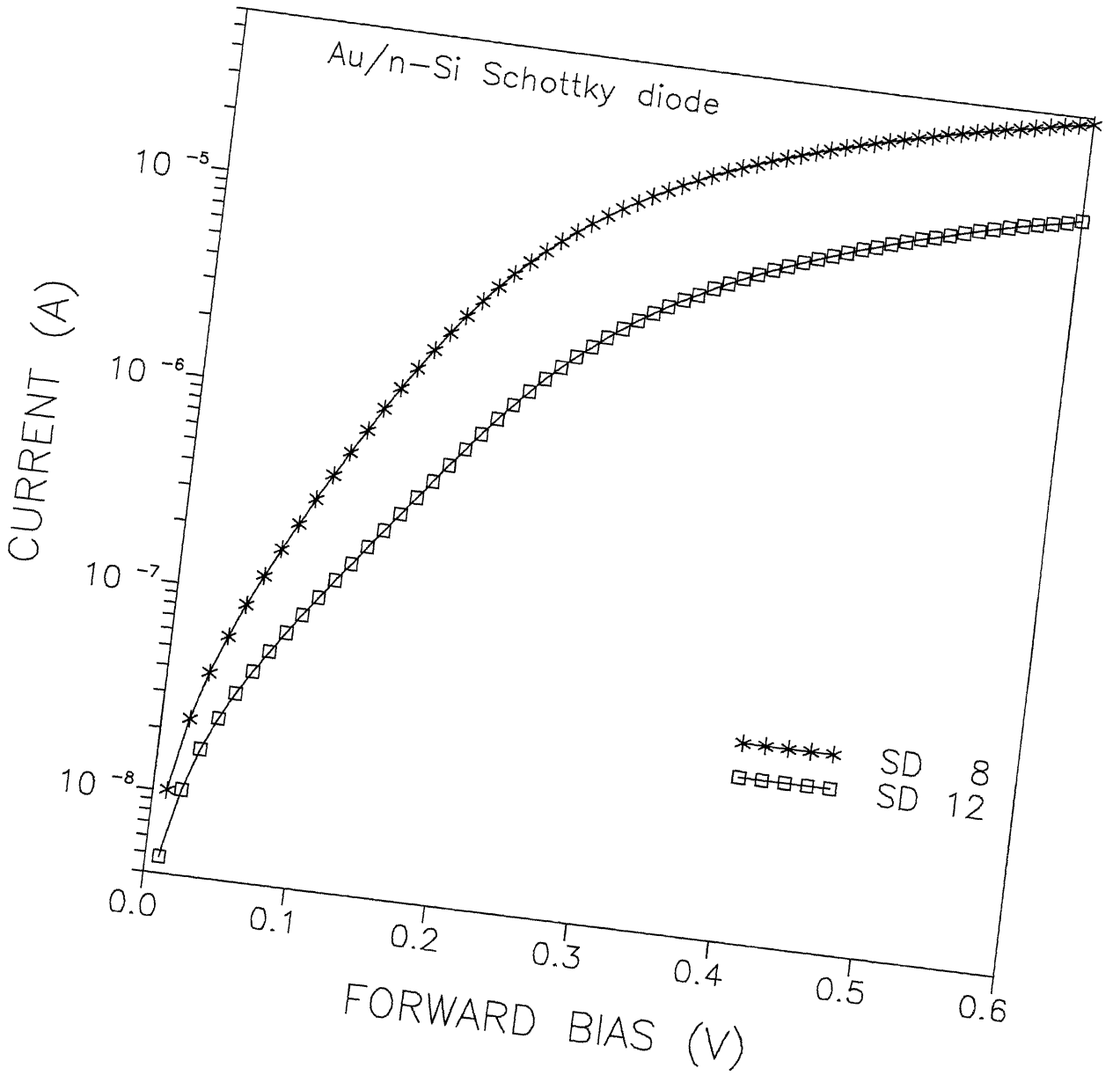

Fig. 3.2 Forward Current-Voltage (I-V) characteristics of Au/n-Si Schottky barrier diodes at room temperature.

R_s in steps. Iteration continues until one finds a set of I_s, η, and R_s values which fit the experimental data over as wide range of forward bias as possible with minimum deviation.

3.1.1 Zero bias barrier height

The zero bias barrier height ϕ_{bo} is obtained by substituting the values of I_s, diode area $A_d = 7.85 \times 10^{-7} m^2$ (corresponding to 1 mm diameter) and effective Richardson constant $A^{**} = 1\ 12 \times 10^6 Am^{-2}K^{-2}$ for n-type silicon [1] in eq.(1.7). The values of ϕ_{bo} obtained together with the ideality factor η and series resistance (R_s) determined by iteration for various diodes are listed in Table 3 1. Clearly, there is variation in ϕ_{bo} values from 0.72 to 0 79 V. Further, the diodes fabricated can be divided into two groups :

(i) exhibiting values of η in the range 1.16 - 1.66 with corresponding R_s varying from 213 - 392 Ω.

(ii) having high ideality factor and series resistance in excess of 3000 Ω.

The characteristics of the latter group can possibly be attributed to the presence of an interfacial oxide layer either formed during the fabrication steps because of the poor vacuum or could not be removed completely during the etching operation.
The high ideality factor essentially means that less current is flowing through the Schottky diode. The variation of the zero-bias barrier height can be explained on the basis of barrier inhomogeneities. As reported earlier by Werner and Guttler [40] and Chand and Kumar [20], the diodes invariably exhibit barrier inhomogeneities, which can be described by a Gaussian distribution function. Also, the value of zero-bias barrier height measured from I-V characteristics correspond to apparent barrier height which depend on the mean and standard deviation of the distribution funtion and temperature. The values of the ϕ_{bo} listed in Table 3.1, in fact, are for diodes fabricated in different batches. These diodes are likely to exhibit variation in the mean and the standard deviation. The recombination of the electrons and holes in the depletion region is also reported to influence the total current of the Schottky diodes with high barrier [9,10]. Such a process normally takes place effectively via localized centres with energies lying near the middle of the band gap [8,41]. According to chen et al. [34], if the recombination mechanism contributes 30% to the total current at room temperature an apparent decrease of barrier height by lomer

Table 3.1: Diode Parameters as obtained for Au/n-Si (111) Schottky barrier from I-V and C-V measurements.

Diode Name	I_s(nA)	R_s (Ω)	η	ϕ_{bo} I-V measurement	ϕ_{bo} C-V measurement	Diff. in ϕ_{bo}
sd1	1.06	213	1.16	0.79	0.84	0.05
sd2	26.51	632	1.26	0.74	—	—
sd3	3.59	397	1.59	0.79	0.81	0.02
sd4	4.52	302	1.24	0.79	0.84	0.05
sd5	4.53	268	1.32	0.79	0.85	0.07
sd6	4.52	248	1.66	0.79	0.91	0.12
sd7	25.01	4949	1.53	0.75	1.57	0.82
sd8	25.91	5627	1.35	0.74	1.08	0.34
sd9	22.03	6392	1.72	0.75	1.02	0.27
sd10	53.26	6847	1.86	0.72	1.06	0.33
sd11	13.47	3247	1.42	0.76	1.05	0.29
sd12	14.21	4313	1.94	0.76	1.09	0.33

should occur, if the contribution is 99 9% at 200 K, barrier height appears reduced by 0 12V. However, recombination saturation-current (I_{ro}) estimated using eq.(1.14) for n-type silicon with $n_i = 10^{16}m^{-3}$, $\tau = 10^{-6}s$, depletion width w = 0.3μm and diode area $A_d = 10^{-7}m^2$ comes out to 2.4×10^{-11}A. This current is two orders of magnitude smaller than the saturation current found in the Au/n-Si (111) Schottky diodes at 300 K. It can therefore be said that recombination process is not all influencing the diode current and hence the barrier height in the present case. Instead, barrier inhomogenieties seem to be responsible for the observed changes in the barrier height. The real test is, of course possible by measuring the I-V characteristics over a wide range of temperature below 300 K and extracting the value of mean and standard deviation of the distribution function. Such studies are expected to show different values of mean barrier height ϕ_{bo} and the standard deviation. Needless to say, the barrier height of 0.79 V found at 300 K for some schottky diodes is in excellent agreement with findings of chen et.al [34], whose value of ϕ_{bo} is 0.08 V at room temperature.

3.2 Barrier height by C-V measurement

The barrier height of Au/n-Si(111) Schottky diodes has also been determined by measuring the capacitance under the reverse bias condition. Figs. 3 3 and 3.4 show $1/C^2$ verses V plot for various diodes. Such a plot yields a straight line as per eq (1.19) with the intercept V_{Ro} on the voltage axis giving the barrier height as

$$\phi_b^{CV} = V_{Ro} + \phi_n + kT/q \tag{3.1}$$

where

$$\phi_n = \frac{kT}{q} ln(\frac{N_C}{N_D}) \tag{3.2}$$

The barrier height evaluated for various diodes in this manner are listed in Table 3.1. We see that these values are invariably higher than those obtained from the I-V data. Moreover, there are still two groups of diodes as pointed out earlier. This result is in consonance with the findings of other workers [40,42]. The discrepancy has been attributed to the inhomogeneities in the barrier height itself. Werner and Guttler [40] solved the C-V equation analytically by incorporating a Gaussian distribution function for the barrier height inhomogeneities and shown that ϕ_b^{CV} correspond to mean itself

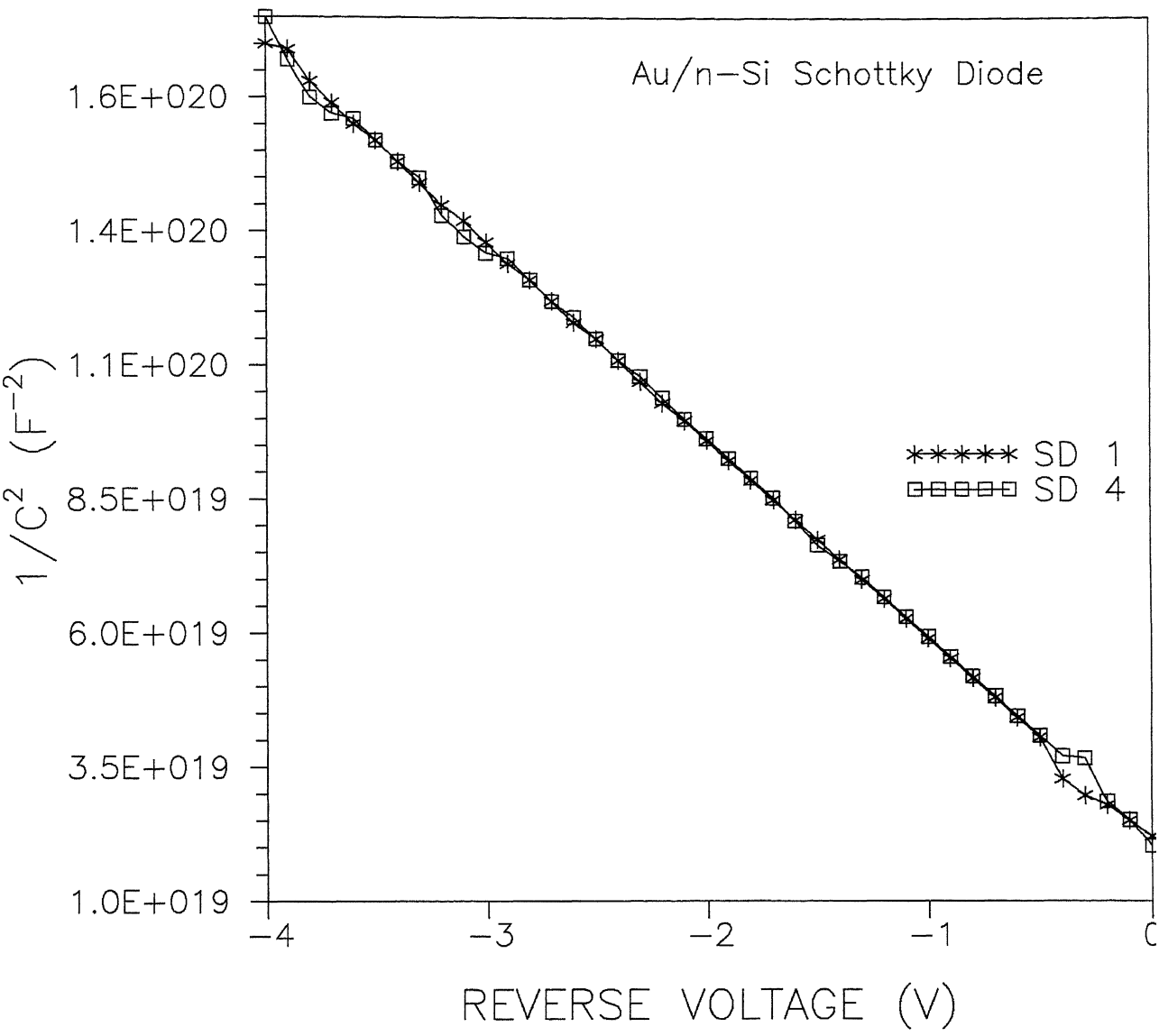

Fig. 3.3 $1/C^2$ versus Voltage plots for Au/n-Si Schottky barrier diodes.

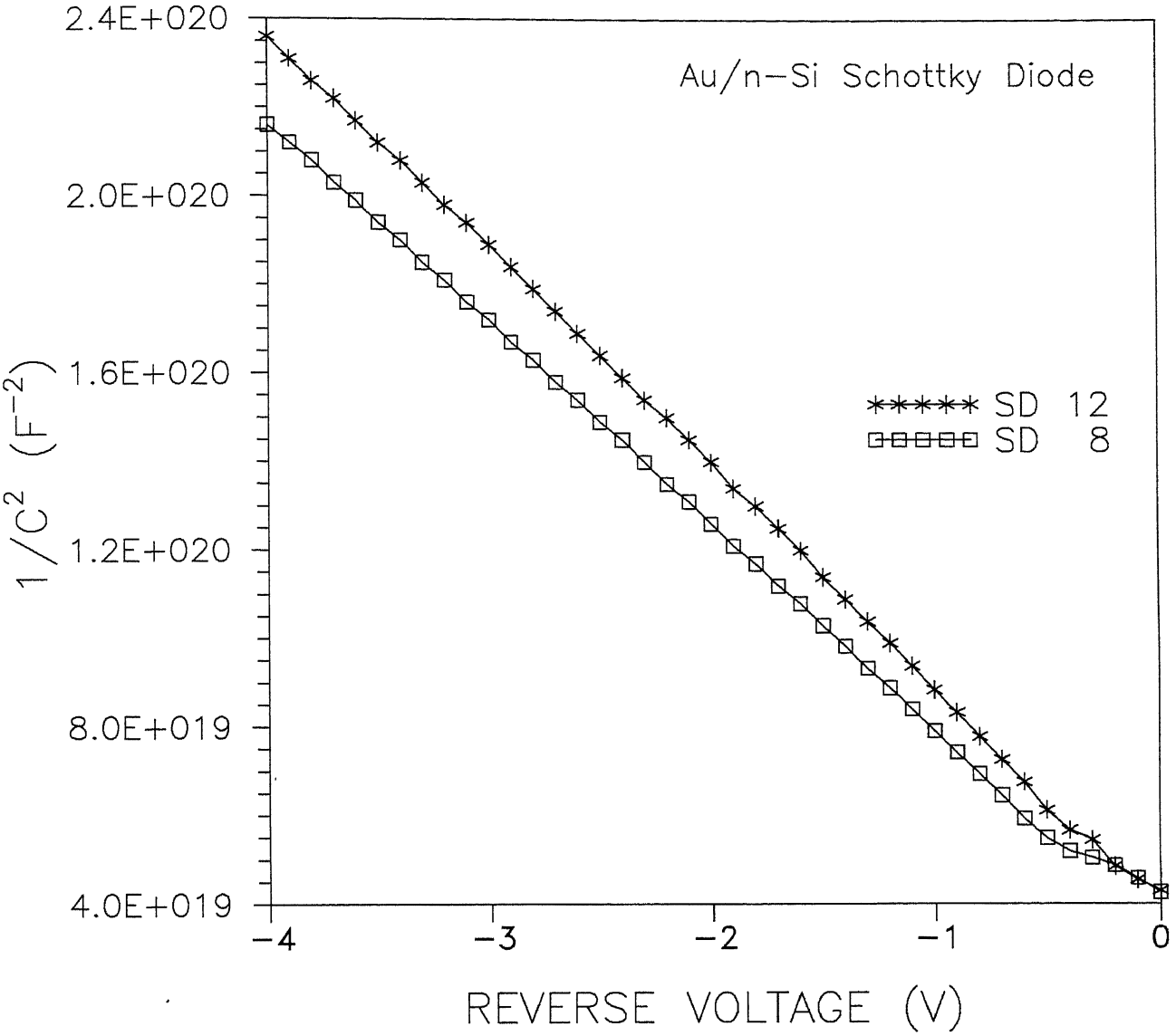

Fig. 3 4 $1/C^2$ versus Voltage for Au/n-Si Schottky barrier diodes.

3.3 X-ray diffraction

Fig.3 5 shows the X-ray diffraction patterns of Au/n-Si (111) Schottky barrier diode samples prior to (a) and after (b) annealing at $450°C$ for 30 minutes. The diffraction peaks of both the patterns correspond to gold metal. Also, as deposited gold film on n-Si (111) exhibits a single diffraction peak amounting to preferred orientation of grains However, on annealing an usual powder diffraction pattern results which means that randomly oriented bigger grains have emerged The 2θ, interplanar spacing d ($\AA$), indices of reflection (hkl) for both the patterns are given in Table 3.2.

3.4 RBS and SEM studies

In order to get insight about the nature of the interface region of Au/n-Si schottky barrier diodes, Rutherford backscattering spectrometry (RBS) experiments were performed in a manner described in section 2.4. Fig. 3 6 shows the scattering yield of ions as a function of energy for samples in which gold film was deposited onto n-Si substrate. There is a sharp peak at $\approx 1.2MeV$ that corresponds to gold species. The nature of peak suggests that gold is concentrated in a very narrow region in terms of thickness. The RBS spectrum is also simulated using the code RUMP [43]. The geometry and sample structure used for simulation is shown in Fig 3.7. The simulated spectrum depicted by solid line in Fig. 3.6 matches very well with the experimental one. It indicates that there is no reaction at the gold-silicon interface, which appears sharply defined. Fig. 3.8 shows the spectrum after annealing of the sample at $450°C$ for 30 min. Notice reduction of the peak at 1.2 MeV and emergence of a tail at lower energies. Such an observation generally indicates diffusion of gold species into silicon and/or formation of gold globules during the annealing process. For better comparison the RBS results are presented together in Fig.3.9. Notice that the peak height is reduced to nearly one third. Fig. 3.10 shows typical scanning electron micrographs of Au/n-Si schottky diodes prior to and after annealing at $450°C$ for 30 min. While Fig. 3.10a reveals no structure and possibly giving the topography of the silicon surface itself, Fig. 3.10b is clearly depicting formation of globules, in agreement with the findings of RBS studies discussed above and also reported by Campisano etal. [44]. Obviously agglomeration of gold occured during annealing step. Besides there is

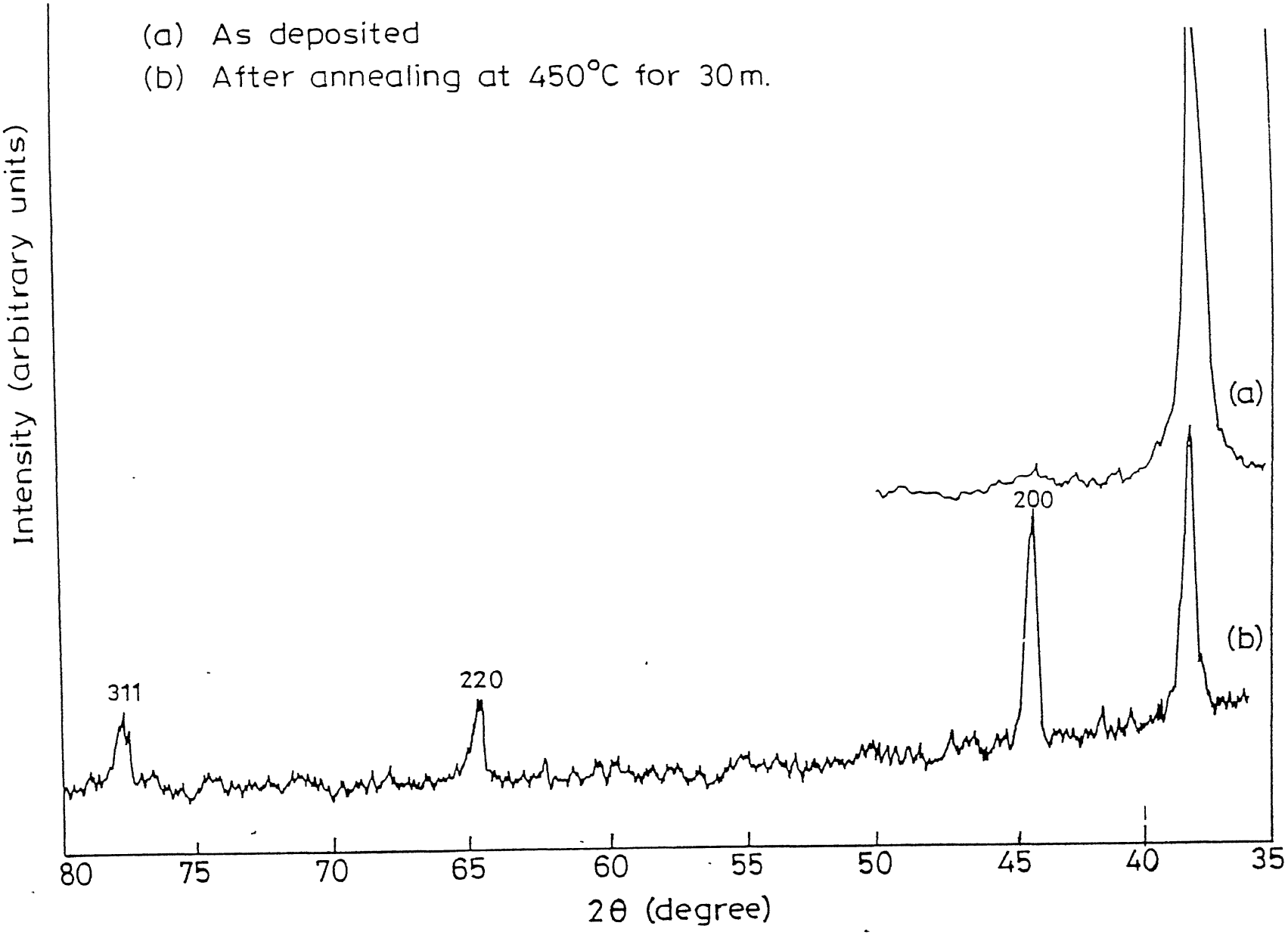

Fig. 3.5 X-ray diffraction pattern of the Au/n-Si Schottky barrier diode :(a) as fabricated and (b) after annealing at 450°C for 30 min.

Table 3.2. Crystal data of Au/-nSi Schottky barrier diodes.

Sample	Peak No.	2θ	d	hkl	Identification
Au/n-n^+-Si(111) as deposited	1	38.1	2.368	(111)	Au
Au/n-n^+-Si(111) annealed at 450°C for 30 minutes	1	38 2	2 356	(111)	Au
	2	44 4	2.040	(200)	Au
	3	64.7	1.441	(220)	Au
	4	77.6	1.230	(311)	Au

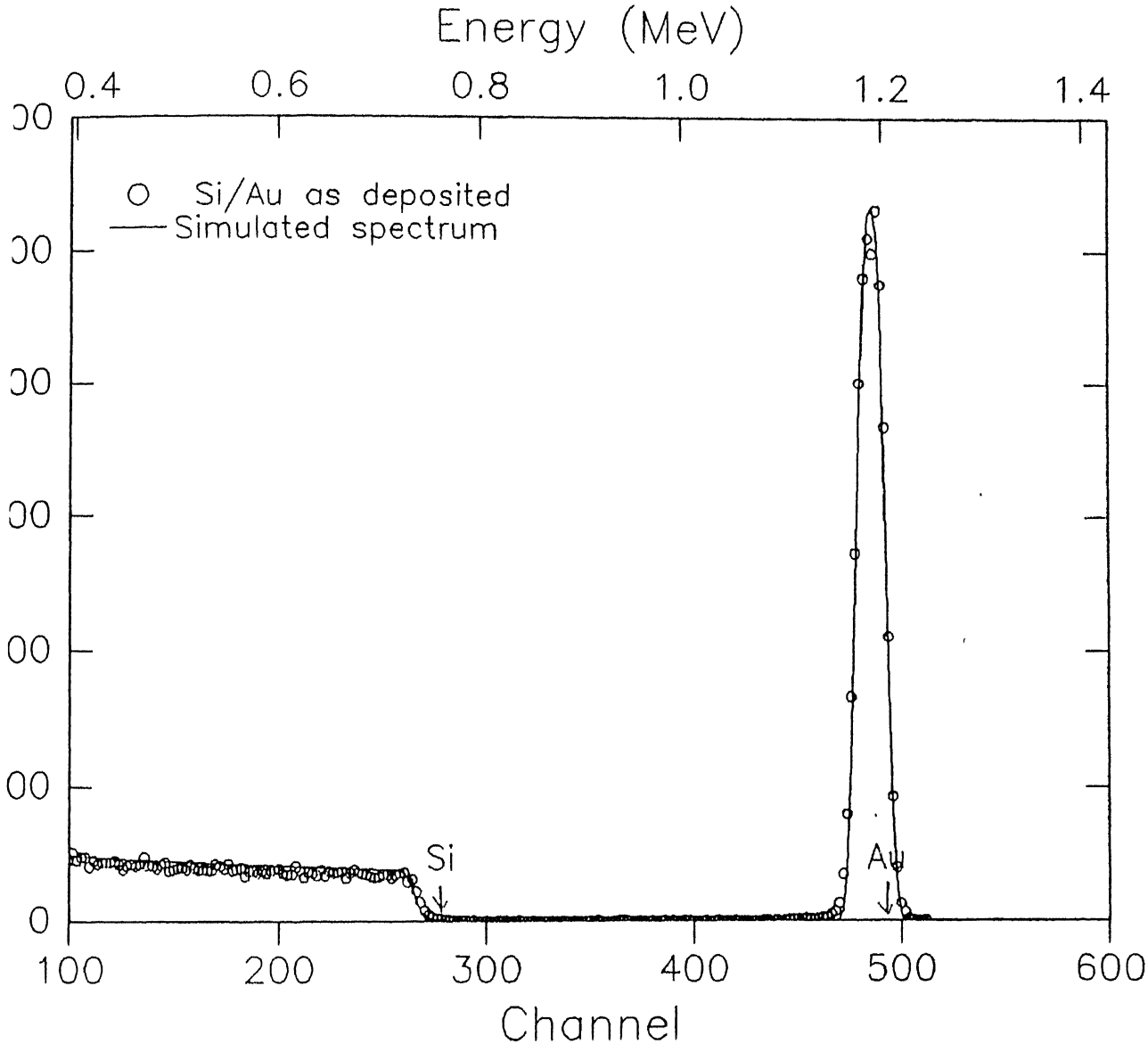

Fig. 3.6 Rutherford backscattering spectrum of Au/n-Si Schottky barrier diode.

```
ılename:     c:\rump\sp37\sp3783.rbs
lentifier:    Si/Au as deposited
[CT Text:    3783
ıte:         Date and time to be entered
ɜam:         1.300 MeV      4He+      2.00 uCoul    @  8.0 nA
ɜometry:     IBM       Theta:     0.0  Phi:    30.0  Psi:     0.0
]A:          Econv:    2.064   187.600    First chan:  1.0   NPT:   512
ɜtector:     FWHM: 14.0 keV   Omega: 2.570
ɔrrection:   1.1500
#     Thickness          Sublayers      Composition  . . .
 1     200.00 A             auto          Au   1.000
 2   20000.00 A             auto          Si   1.000
================================================================================
i   Z=14   Mass= 28.086   K(He)=0.5853   Energy= 760.9 keV   Channel= 277.805
ı   Z=79   Mass=196.970   K(He)=0.9270   Energy= 1.205 MeV   Channel= 493.007
ɾe I am!
ɾe I am!
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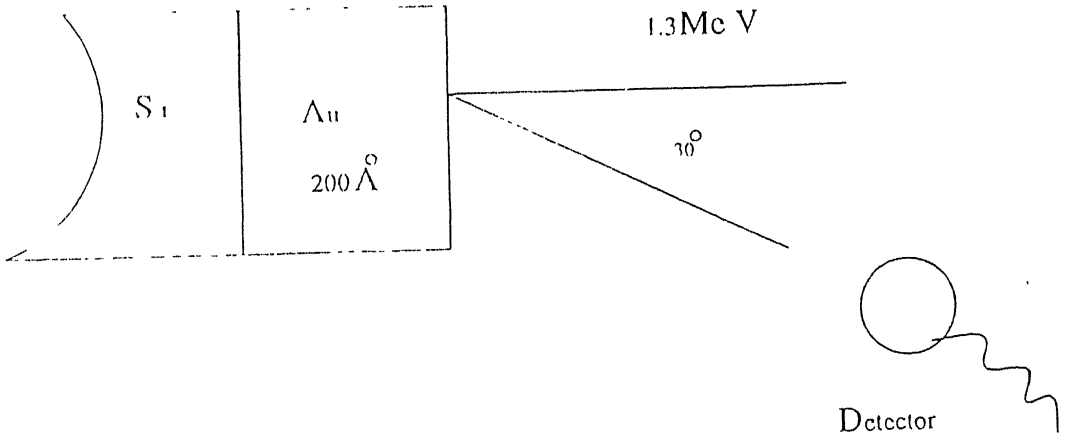


Fig. 3.7 Rutherford backscattering spectrometry (RBS) geometry and structure used for simulation.

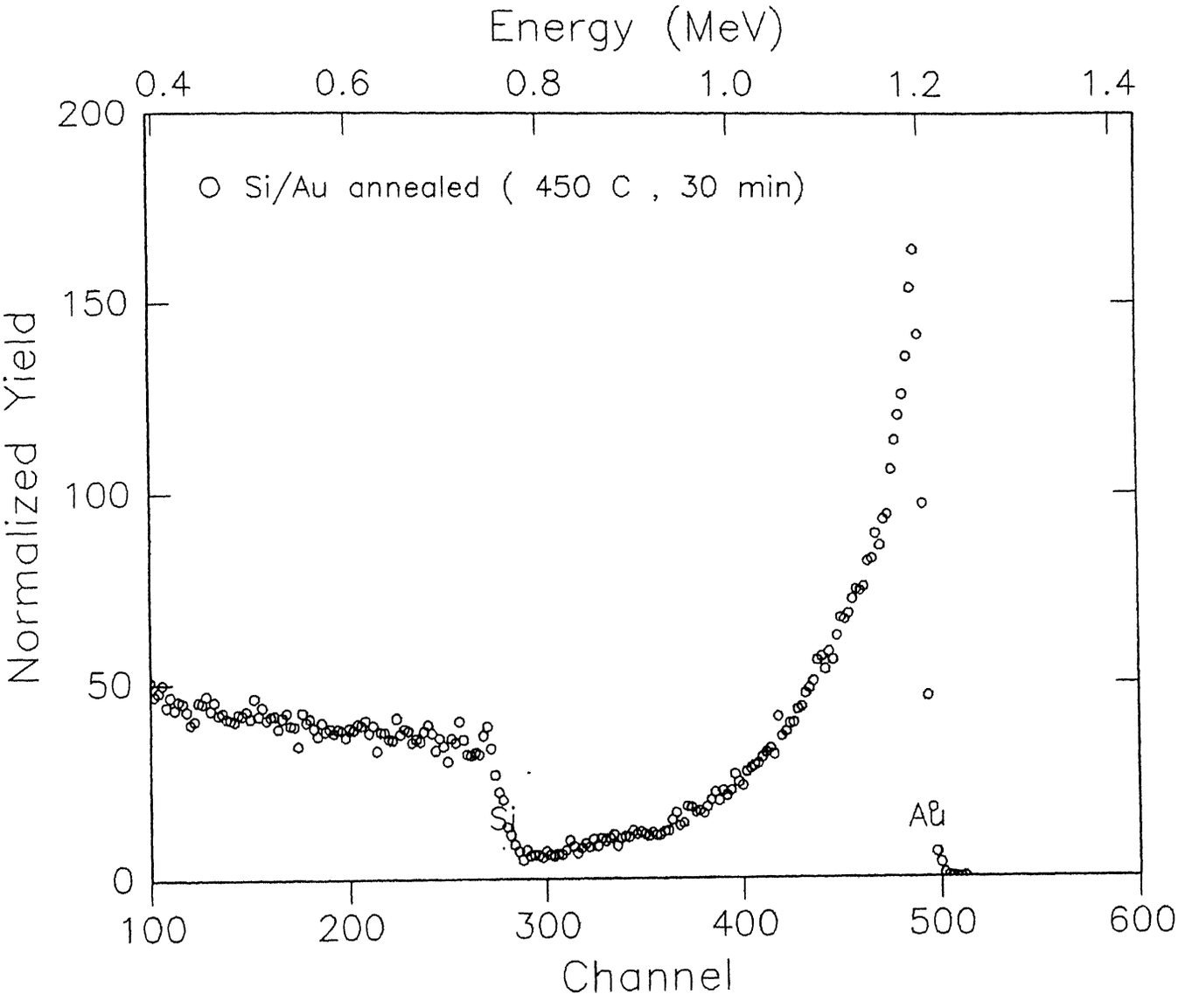


Fig. 3.8 Rutherford backscattering spectrum of Au/n-Si Schottky barrier diode after annealing at 450°C for 30 min.

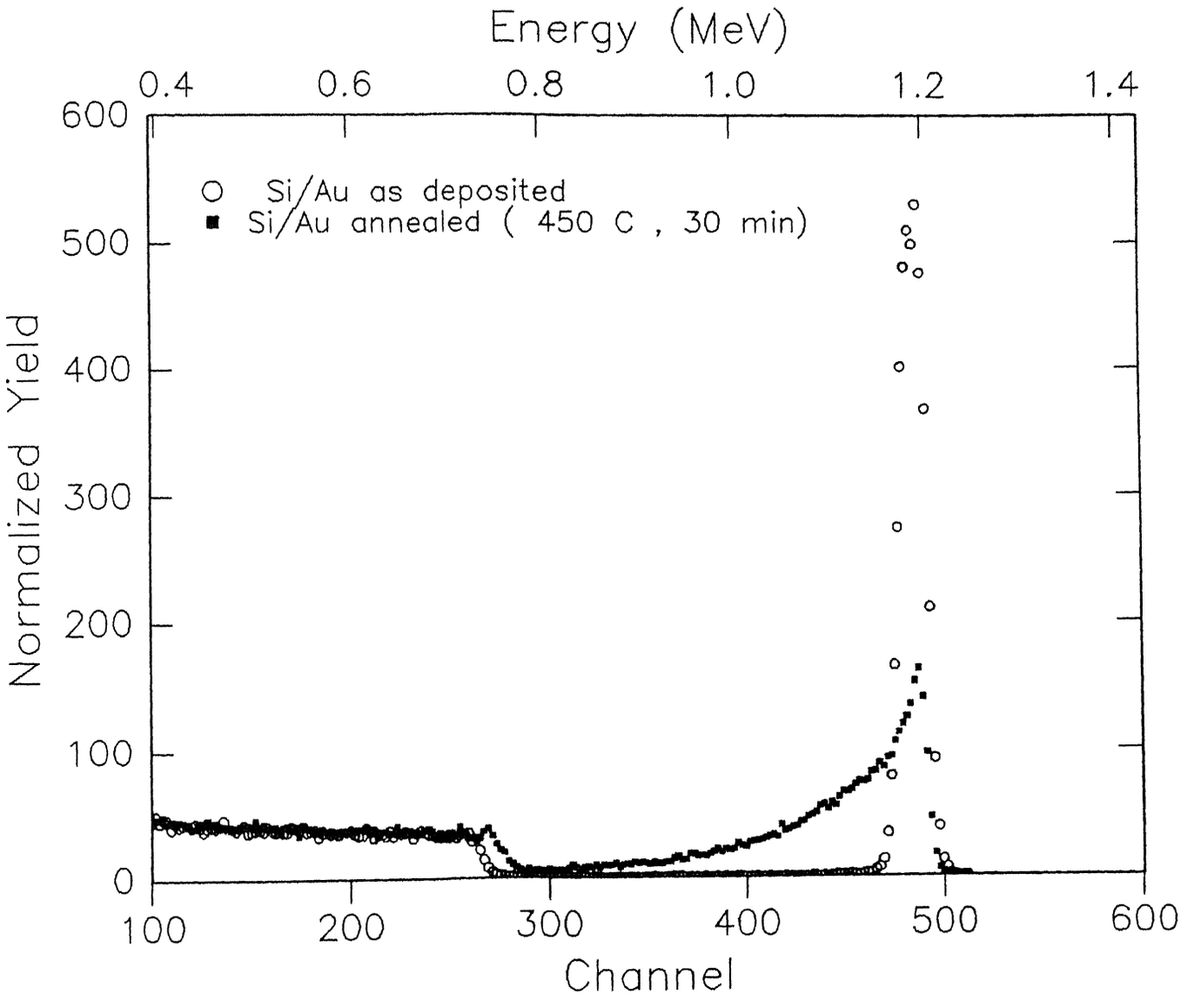
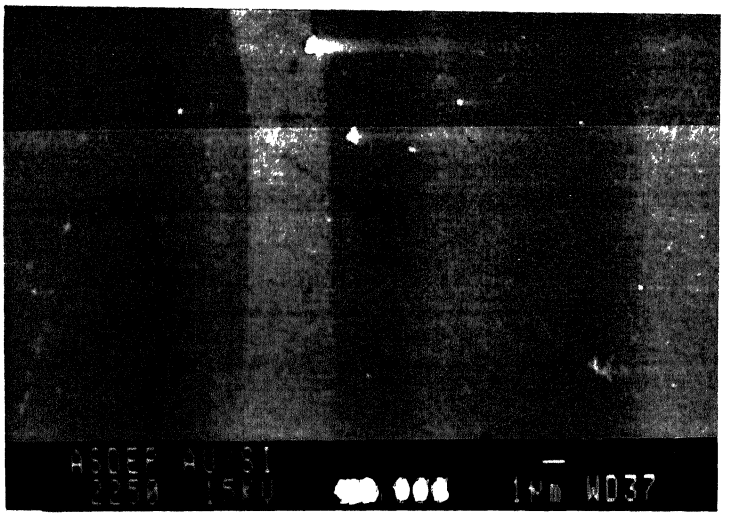
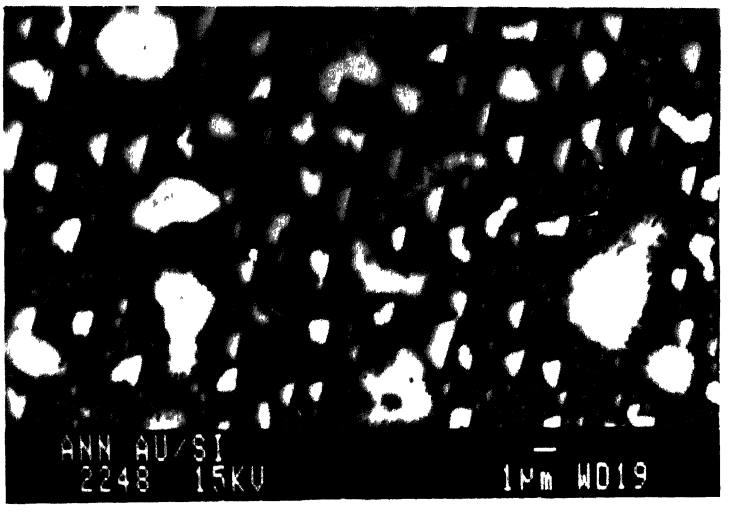


Fig. 3.9 Rutherford backscattering spectra of Au/n-Si Schottky barrier diode prior to (.....) annealing and after annealing (—) at 450°C for 30 min, i.e., Figs 3 7 & 3.8 superimposed.



(a)



(b)

Fig. 3 10 Scanning electron micr· graph of Au/n-Si Schottky barrier diodes showing microstructure : (a) prior to and (b, after annealing at $450°C$ for 30 minutes. Notice emergence of globules in (b).

possibility of some diffusion of gold taking place into the silicon substrate. Formation of gold globules is the reason perhaps for deterioration in the characteristics of the Schottky diodes.

Chapter 4

Simulation studies

4.1 Basic equations :

The Schottky diode parameters, namely barrier height ϕ_b and ideality factor η are found to exhibit abnormal behaviour at low temperatures. Accordingly, barrier height decreases while ideality factor increases with decrease in temperature. The existence of barrier height inhomogeneities at the metal- semiconductor interface can explain satisfactorily the observed characteristics [44-50]. The barrier height inhomogeneities may result due to variation in the thickness of the deposited metal, non-uniformity of the interfacial charges and/or locally defective hot regions [51]. The Gaussian distribution function that describes the barrier inhomogeneities adequately has the form [40,41,51,52].

$$P(\phi_b) = \frac{1}{\sigma\sqrt{2\pi}} exp[-(\frac{(\phi_b - \bar{\phi_b})^2}{2\sigma^2})] \tag{4.1}$$

where the term $1/\sigma\sqrt{2\pi}$ is called normalization constant, $\bar{\phi_b}$ the mean barrier height and σ is the standard deviation.

The total current through a Schottky diode is then given by

$$I(V) = \int_{-\infty}^{+\infty} I(\phi_b, V) P(\phi_b) d\phi_b \tag{4.2}$$

where $I(\phi_b, V)$ is the current for a barrier of height ϕ_b at a forward bias of V volts. According to Chand & Kumar [20], final expression for I(V) based on the thermionic emission-

diffusion (TED) theory becomes

$$I(V) = A_d A^{**} T^2 exp[\frac{-q}{kT}(\bar{\phi_b} - \frac{\sigma^2 q}{2kT})]exp(\frac{qV}{kT})[1 - exp(\frac{-qV}{kT})] \tag{4.3}$$

Further, assuming linear voltage variation of the distribution parameters, mean barrier height $\bar{\phi_b}$ and standard deviatın σ, we can write

$$\bar{\phi_b} = \bar{\phi_{bo}} + \gamma V \tag{4 4}$$

and

$$\sigma = \sigma_o + \xi V \tag{4.5}$$

Where $\gamma = (\frac{\partial \bar{\phi_b}}{\partial V})$ and $\xi = (\frac{\partial \sigma}{\partial V})$ are positive voltage co-efficients. Making these substitutions into eq.(4.3) and neglecting the $\xi^2 V^2$ term, we get

$$I(V) = I_s exp(\frac{qV}{kT\eta_{ap}})[1 - exp(\frac{-qV}{kT})] \tag{4 6}$$

where

$$I_s = A_d A^{**} T^2 exp(\frac{-q\phi_{ap}}{kT}) \tag{4 7}$$

stands for the saturation current Here ϕ_{ap} and η_{ap} represent the apparent barrier height and standard deviation and are given by

$$\phi_{ap} = \bar{\phi_{bo}} - \frac{\sigma_o^2 q}{2kT} \tag{4.8}$$

$$\frac{1}{\eta_{ap}} = (1 - \gamma) + \frac{\sigma_o q \xi}{kT} \tag{4.9}$$

Eq.(4.6) ıs of the form of current expression resulting due to TED mechanism from a homogeneous barrier and has ϕ_{ap} and η_{ap} in place of ϕ_{bo} and η, respectively (compare, e.g., with eq.(1.6)).

4.2 Simulation of diode parameters

Simulation is mainly undertaken to study the changes caused by various parameters (σ_o, γ, ξ) on the barrier height vs. temperature, ideality factor vs. temperature and $\ln(I_S/T^2)$ vs. $1/T$ characteristics. The simulated plots can be very useful in the analysis of experimentally measured I-V data. Since, in simulation, we purposely vary some parameters and observe their effects, ascertaining the reason for a particular feature observed experimentally becomes possible.

4.2.1 Barrier height

Eq.(4 8) is used to simulate the apparent barrier height (ϕ_{ap}) by varying the value of the standard deviation (σ_o), i.e, increasing the extent of barrier inhomogeneities. While the value of $\bar{\phi_{bo}}$ selected is 0.80 V (known for Au/n-Si Schottky diode at 300K), σ_o is varied in the range zero to 0 10 with a step of 0.02. Fig. 4.1 shows ϕ_{ap} as a function of T for various values of σ_o. This clearly shows that the decrease in barrier height is caused by the existence of distribution (i.e, $\sigma_o \neq 0$) and its effect becomes more dominant at low temperatures. Also, for low σ_o, barrier height initially remains constant (or decreases slowly) but decreases sharply below a certain temperature. The place of inflexion moves towards higher temperature as the value of σ_o increases. In other words, bending of the ϕ_{ap} vs T gets initiated earlier (while cooling) if inhomogeneities are severe (i.e, σ_o is high).

4.2.2 Ideality factor

Eq.(4.9) is utilized to simulate the apparent ideality factor (η_{ap}) for various values of the voltage coefficient ξ in the range -.020 to +.020 while fixing σ_o and γ at 0.06 and 0.08, respectively. Fig. 4.2 shows variation of simulated ideality factor (η_{ap}) with temperature for different values of ξ. It clearly reveals that ideality factor (η_{ap}) increases or (decreases) sharply with fall in temperature if ξ is negative (or positive). Since experiments usually subscribe to increase of η_{ap} with decrease in temperature, it is obvious that ξ should essentially be negative. Also, if ξ is zero, η_{ap} assumes a fixed value $\eta = 1/(1-\gamma)$ determined by the voltage coefficient (γ) of the barrier height at all the temperatures. If γ is positive $\eta > 1$ whereas for negative $\gamma's$, $\eta < 1$. Both types of cases have been observed in practice[20,40,54] The latter is meaningful only for negative ξ and $|\gamma| < (|\sigma_o q\xi/kT|)$ as η_{ap} for a real Schottky diode should be greater than unity [20, 40]. Further, it is obvious from Fig.4.2 that ideality factor begins to rise early at high temperature for greater values of negative ξ's. As the temperature increases, the second term of eq. (4.9) becomes less effective and η_{ap} attains a saturation value of $\eta = 1/(1-\gamma)$ Fig. 4.3 illustrates the effect of γ on the ideality factor η_{ap}. Clearly, the curve gets shifted towards higher η_{ap} with increase in the value of γ by a constant factor. Fig. 4 4 shows the influence of σ_o on the ideality factor vs temperature plots. Notice that nature of variation is similar to that found in Fig.4.2. This is due to that fact that ξ and σ_o have similar dependence on η_{ap} in eq.(4.9)

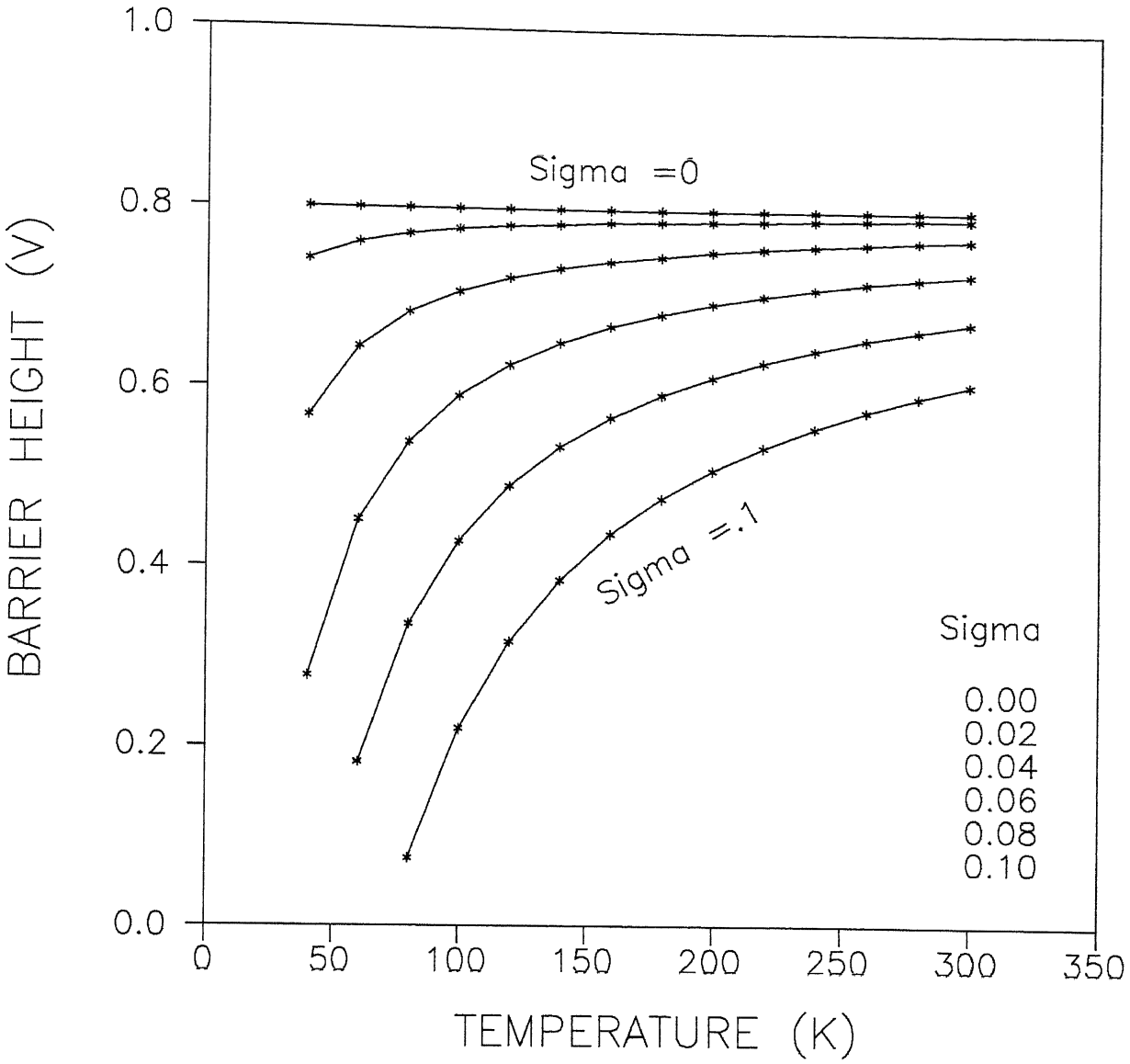


Fig. 4.1 Apparent barrier height (ϕ_{ap}) as a function of temperature for various values of standard deviation (σ_o), assuming $\phi_{bo} = 0.8V$

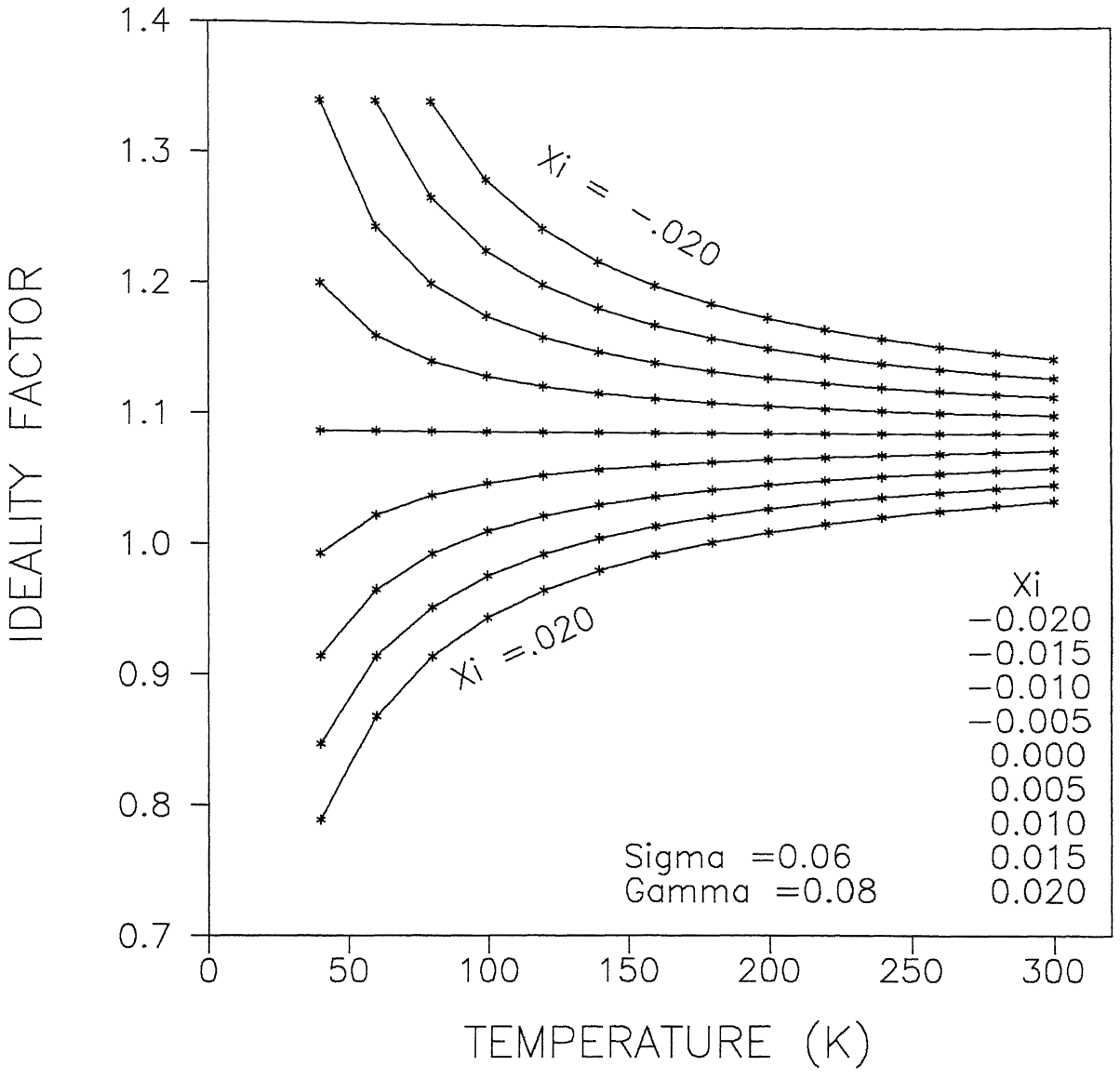


Fig. 4.2 Ideality factor (η) as a function of temperature for various values of voltage coefficient (ξ), assuming zero-bias standard deviation $\sigma_o = 0.06$ and voltage coefficient ($\gamma = 0.08$).

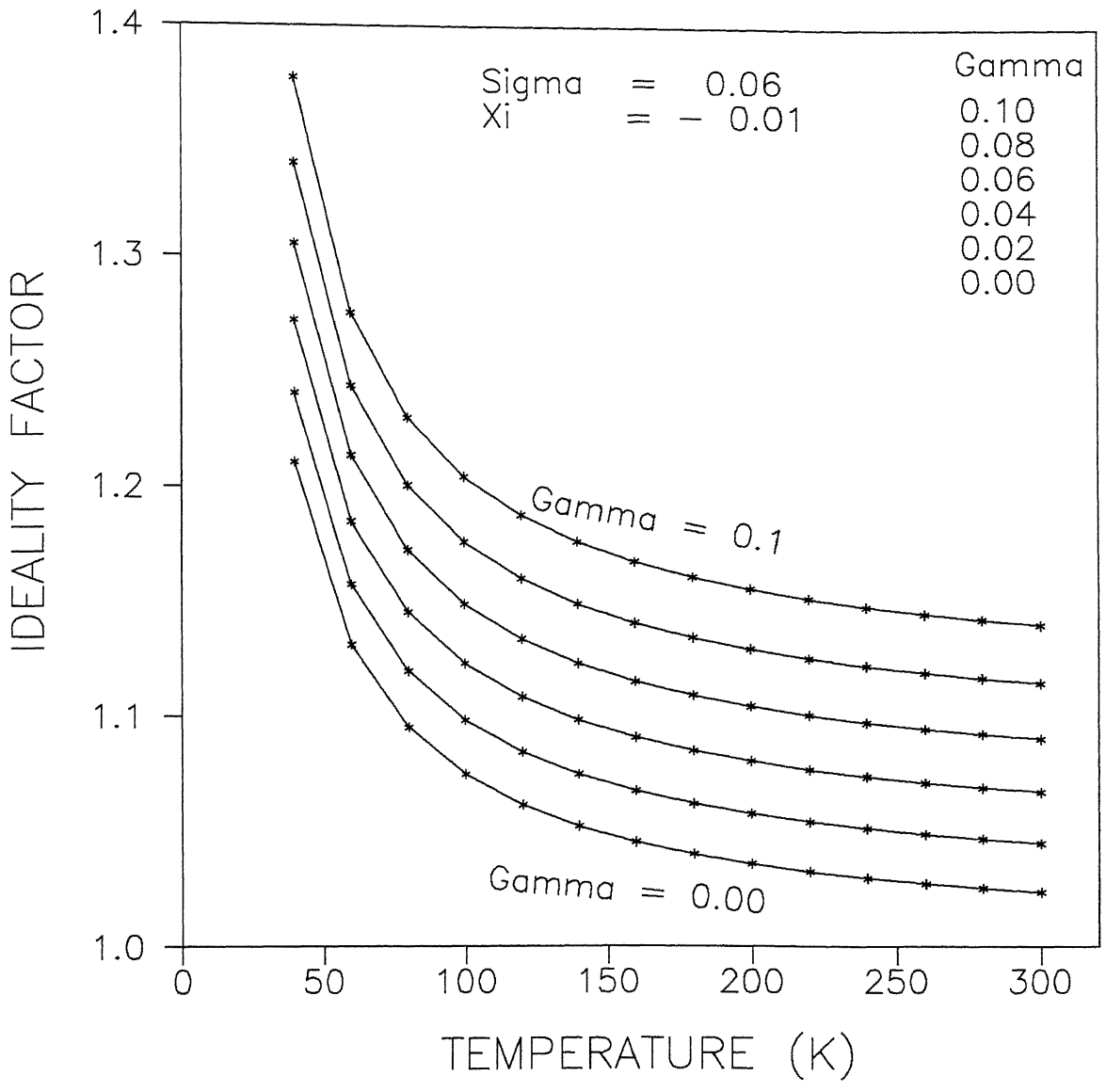


Fig. 4.3 ideality factor (η) as a function of temperature for various values of voltage coefficient (γ) assuming zero-bias standard deviation $\sigma_o = 0.06$ and voltage coefficient $\xi = -0.01$.

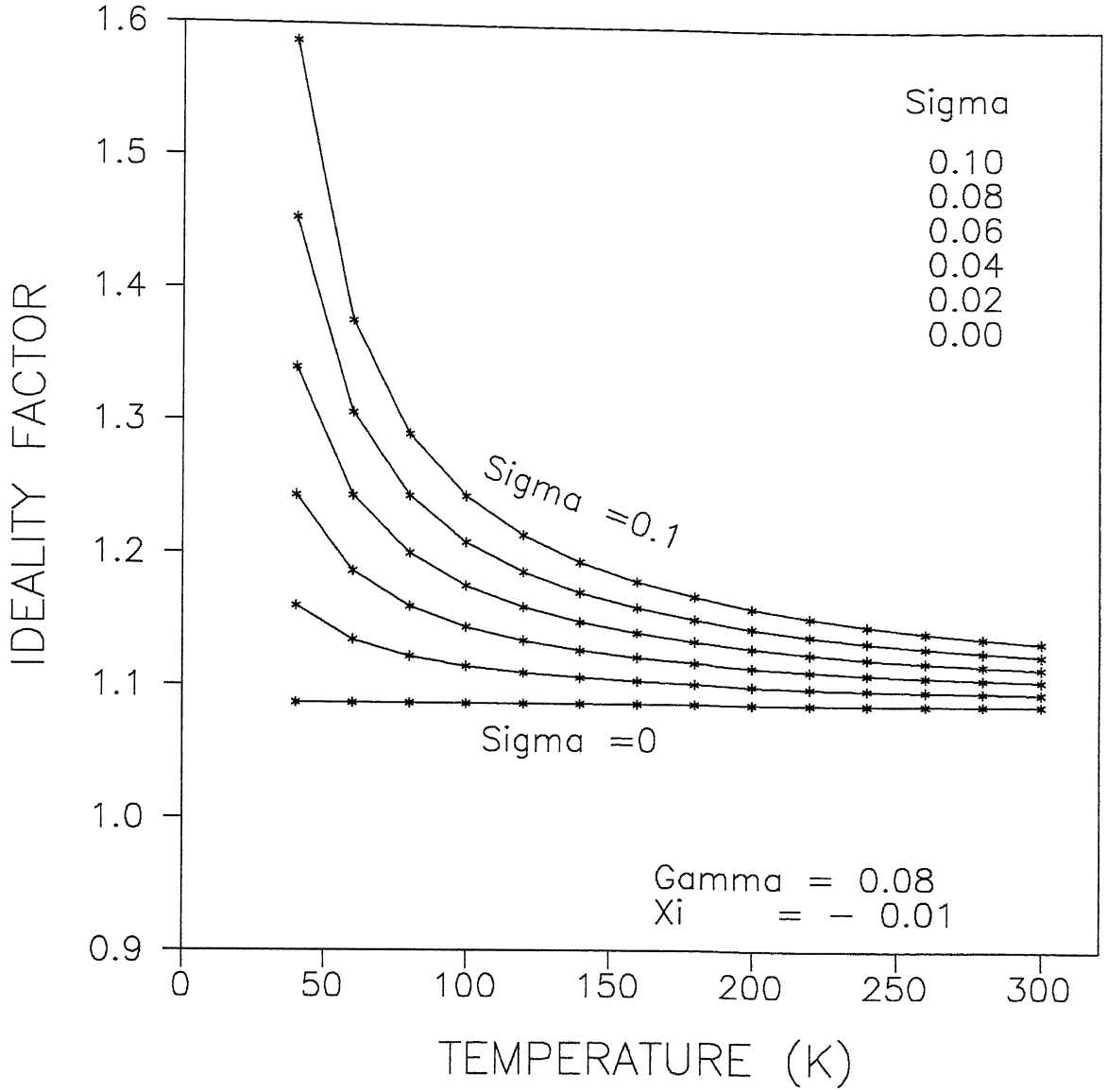


Fig. 4.4 Idealıty factor (η) as a function of temperature for various values of the standard deviation assuming voltage cofficient γ and ξ as 0.08 and 0.01 , respectively.

4.2.3 Saturation current

Fig 4.5 shows the $\ln(I_s/T^2)$ vs 1000/T plot simulated using eq.(4.7) by taking $\bar{\phi_{bo}} = 0.80$V and σ_o between zero and 0.08. It demonstrates that for $\sigma_o = 0$, i.e., for a homogeneous single barrier, the so called Arrheneous plot is a straight line, whose slope just corresponds to $\bar{\phi_{bo}} = 0.80$V. However, as barrier inhomogeneities (i.e., standard deviation of the Gaussian distribution) increases the plot deviates from linearity in the progressive manner - a result usually observed in practice [20,40]. The activation energy is therefore not uniquely defined.

4.2.4 Total diode current

Most of the resistance in the Schottky barrier diode is attributed to the neutral region of the semiconductor (i.e., between the depletion region and back ohmic contact). The presence of a thin oxide layer and/or impurities are the other sources of resistance. A series resistance R_s is therefore associated for each diode. So, a significant voltage drop occurs across R_s at large forward currents. This amounts to a reduced voltage in the barrier region vis-a-vis actually applied to the terminals of the diode. This is accounted for by replacing V by (V - IR_s) in eq.(4.6). Thus,

$$I = I_s exp(\frac{q(V - IR_s)}{\eta_{ap} kT})[1 - exp(\frac{-q(V - IR_s)}{kT})] \tag{4.10}$$

with I_s as eq.(4.7). Since the current (I) appears on both sides of eq.(4.10), we can not determine its value at any forward bias by simple methods. Hence, use is made here of Newton-Raphson iteration formula. Accordingly, the root of equation f(x) = 0 is given by [55]

$$x = x_o - \frac{f(x_o)}{f'(x_o)} \tag{4.11}$$

Where $f'(x_o)$ denotes the derivative of $f(x)$ at $x = x_o$.

We can define a current function f(I) = 0 using eq.(4.10), such that

$$f(I) = I - I_s exp(\frac{q(V - IR_s)}{\eta_{ap} kT})[1 - exp(\frac{-q(V - IR_s)}{kT})] = 0 \tag{4.12}$$

Introducing parameters $a(= q/kT)$ and $b(= qR_s/kT)$ into L.H.S of eq.(4.12) and rearranging the terms, we get

$$f(I) = I - I_s exp(\frac{aV - bI}{\eta_{ap}}) + I_s exp(aV - bI)(\frac{1}{\eta_{ap}} - 1) \tag{4.13}$$

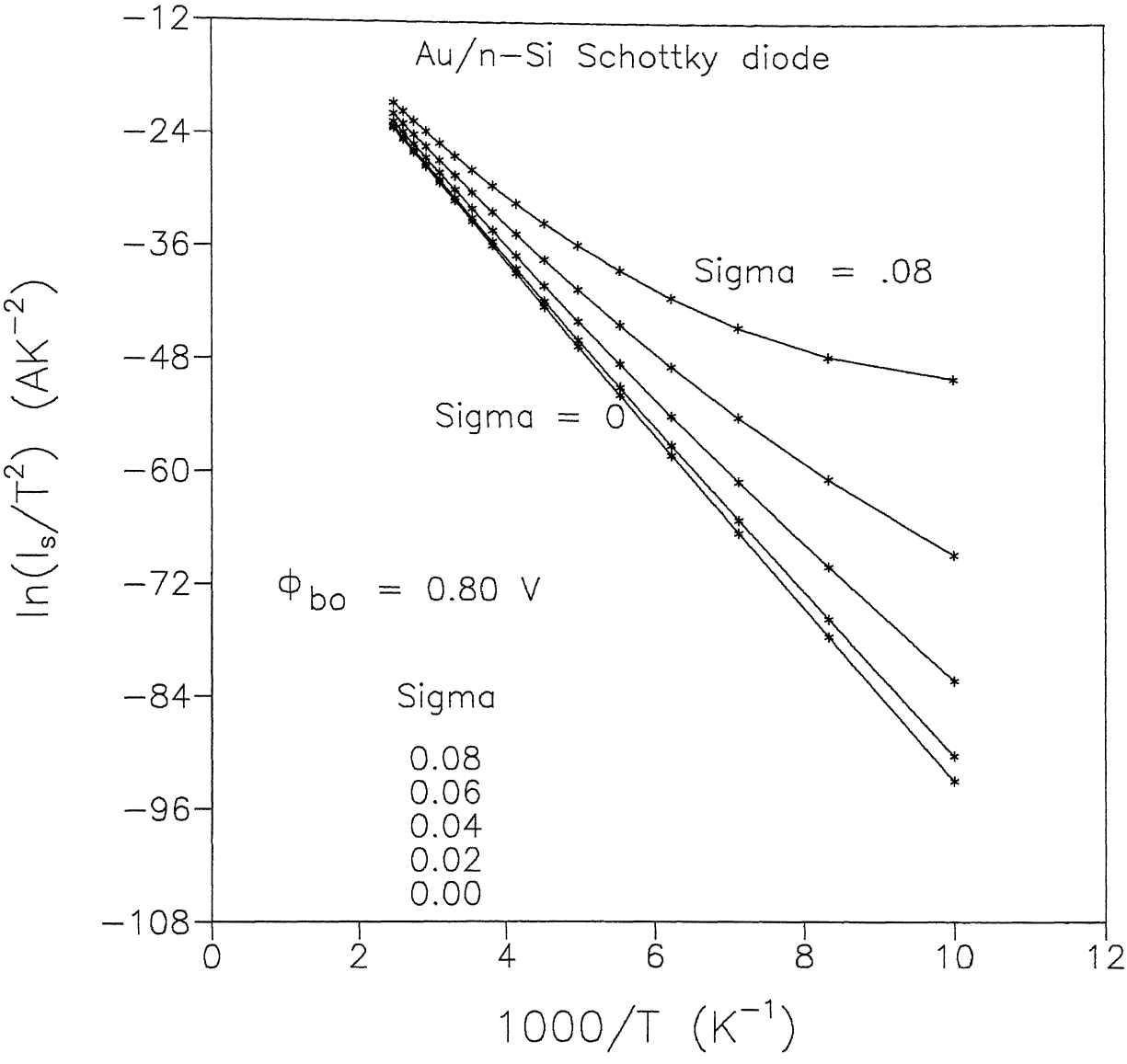


Fig. 4.5 $\mathrm{Ln}(I_s/T^2)$ vs $(1/T)$ plot for various values of zero bias standard deviation (σ_o) assuming zero-bias barrier $\phi_{bo} = 0.8V$.

Differentiating with respect to I, one obtains

$$f'(I) = 1 + \frac{I_s b}{\eta_{ap}} exp(\frac{aV - bI}{\eta_{ap}}) - b(\frac{1}{\eta_{ap}} - 1) I_s exp\{(aV - bI)(\frac{1}{\eta_{ap}} - 1)\} \tag{4.14}$$

Let

$$F_1 = I_s exp(\frac{(aV - bI)}{\eta_{ap}}) \tag{4.15}$$

$$and \qquad F_2 = I_s exp\{(aV - bI)(\frac{1}{\eta_{ap}} - 1)\} \tag{4 16}$$

Eqs.(4.13) and (4.14) can be written as

$$f(I) = I - F_1 + F_2 \tag{4.17}$$

$$f'(I) = 1 + \frac{b}{\eta_{ap}} F_1 - b(\frac{1}{\eta_{ap}} - 1) F_2 \tag{4.18}$$

Applying Newton-Raphson formula (4.11) for current, one writes

$$I = I_o - \frac{f(I_o)}{f'(I_o)} = I_o - \frac{I_o - F_1 + F_2}{1 + \frac{b}{\eta} F_1 - b(\frac{1}{\eta} - 1) F_2} \tag{4.19}$$

where I_o is some reasonable current and $f'(I_o)$ refers to $\frac{df}{dI}|_{I=I_0}$ Using Tailor's expansion for f(I) and retaining first two terms

$$f(I) = f(I_o) + (I - I_o) \frac{\partial f}{\partial I}|_{I=I_0} \tag{4.20}$$

The sketch shown in Fig. 4.6 elaborates the logic behind the iteration method We take some initial guess value I_o and calculate $f(I_o)$. A tangent $f'(I)|_{I=I_0}$ is drawn and extended to meet I-axis at $I = I_1$ (say). We now calculate the value of $f(I_1)$ and draw a tangent$f'(I)|_{I=I_1}$ again cutting I-axis at I_2, so that $f(I_2)$ is found out. This process is repeated until f(I) becomes zero. Needless to say, Newton-Raphson type formula given by eq. (4.11) directly follows from eq. (4 20) since f(I) = 0. Fig 4.7 shows the currents simulated by the method enumerated above for the case of a Schottky diode having $\bar{\phi}_{bo}$= 0.8 V, ideality factor η_{ap}=1 at a temperature of 150 K for various values of series resistance. It reveals that ln(I) vs V plot gives a straight line with R_s= 0 but bends at high currents leading to saturation at any finite R_s. The initiation of bending shifts to lower current and linear portion shrinks with increase in the value of series resistance R_s. That means if current increases rapidly (or slowly) with forward bias, bending should initiate at relatively

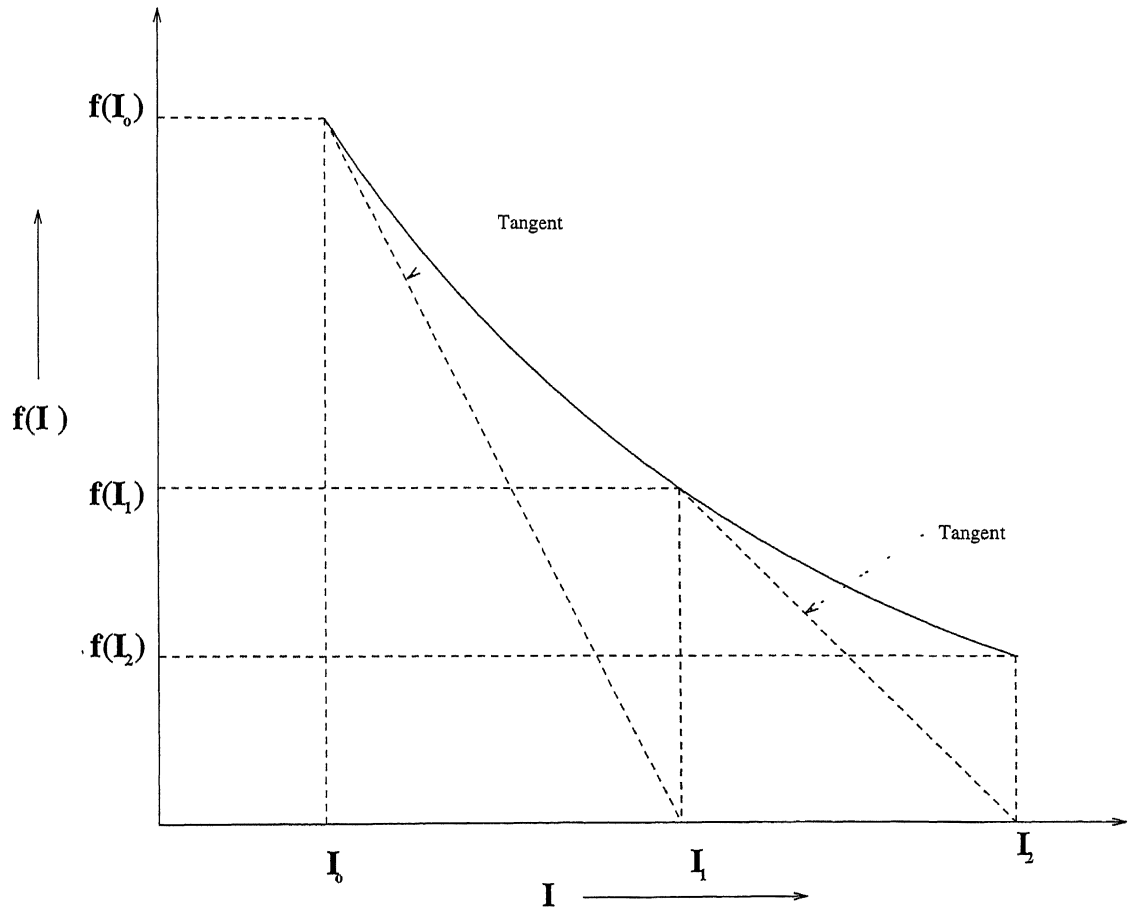


Fig. 4.6 Curve showing iteration method using Newton-Raphson formula for evaluation of simulated current.

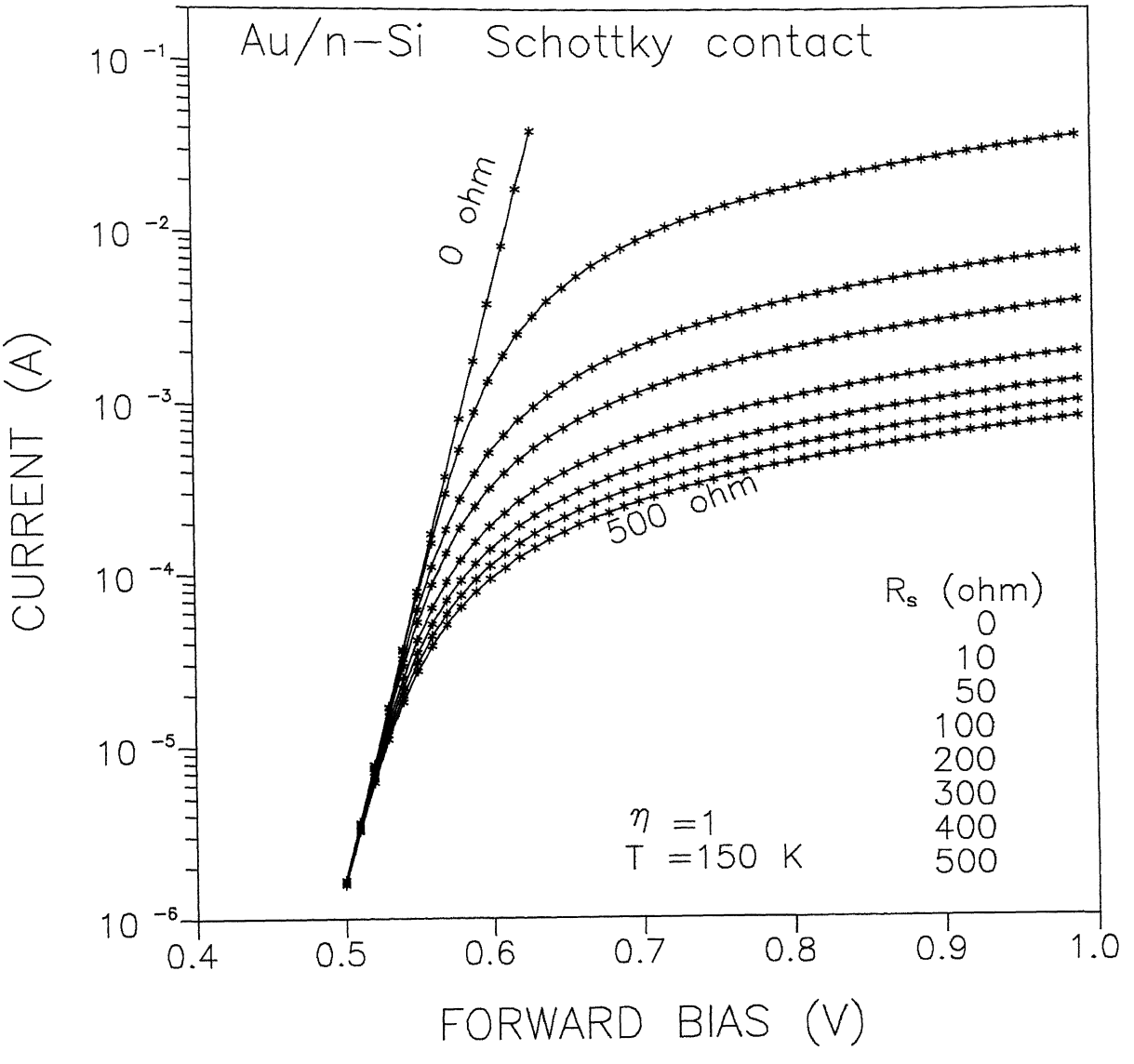


Fig. 4.7 Simulated Current-Voltage characteristics showing effect of series resistance (R_s) at 150 K assuming ideality factor η to be unity.

higher (or lower) voltage. The lower current portion still continues to be a straight line, however The effect of series resistance is basically to limit the current flow through the Schottky diode at higher forward bias. The ln(I) - V characteristics of a Schottky diode having a homogeneous barrier $\bar{\phi_{bo}}$= 0 8 V, η_{ap}=1 and $R_s = 200\ \Omega$ at various temperatures are displayed in Fig. 4 8. The main observation are as follows:

The plot becomes increasingly straight and shifts towards higher bias side as temperature is lowered. The linear portion when extrapolated to zero bias gives ln(I_s) i.e., saturation current. It decreases significantly with decrease in temperature. Further, the bending occurs at the same current level irrespective of temperature. This means that IR_s becomes effective at a particular current for a fixed R_s and therefore bending initiates progressively at higher bias with decrease in temperature. This information coupled with the results shown in Fig. 4.7 suggests that if R_s increases somehow, the bending should initiate at a lower current itself. Fig. 4.9 shows simulated curve of a Schottky diode having barrier height $\bar{\phi_{bo}}$= 0.80 V, and R_s=0 at 200 K for various values of ideality factor. The effect is such that the slope of the straight line decreases with increase in the value of ideality factor. Also, the saturation current remains invariant as it does not depend upon η_{ap}. (see, e.g., eq. 4.7). The nature of plots continues to be similar at other temperatures with values changing appropriately, of course Further, if R_s is given some value, bending starts appearing in ln(I) vs V plots, as shown before in Figs. 4.7 and 4.8. Finally, Fig. 4.10 gives a TED current of a real Schottky diode of parameters: $\bar{\phi_{bo}} = 0.80$ V, $R_s = 200\ \Omega$ at 150 K for various values of ideality factor as obtained by simulation using eq. 4.10 and Newton-Raphson iteration formula. It shows clearly that slope of linear portion of ln(I) vs V plots decreases with increase of ideality factor. Also, bending occurs at the same current level at all temperatures due to a fixed value of the series resistance (R_s). The nature of this plot is very similar to I-V characteristics actually observed and discussed in Chapter 3. Obviously, one can proceed with the interpretation of experimental (I-V) data in the reverse way and determine the barrier parameters together with the level of inhomogeneities present.

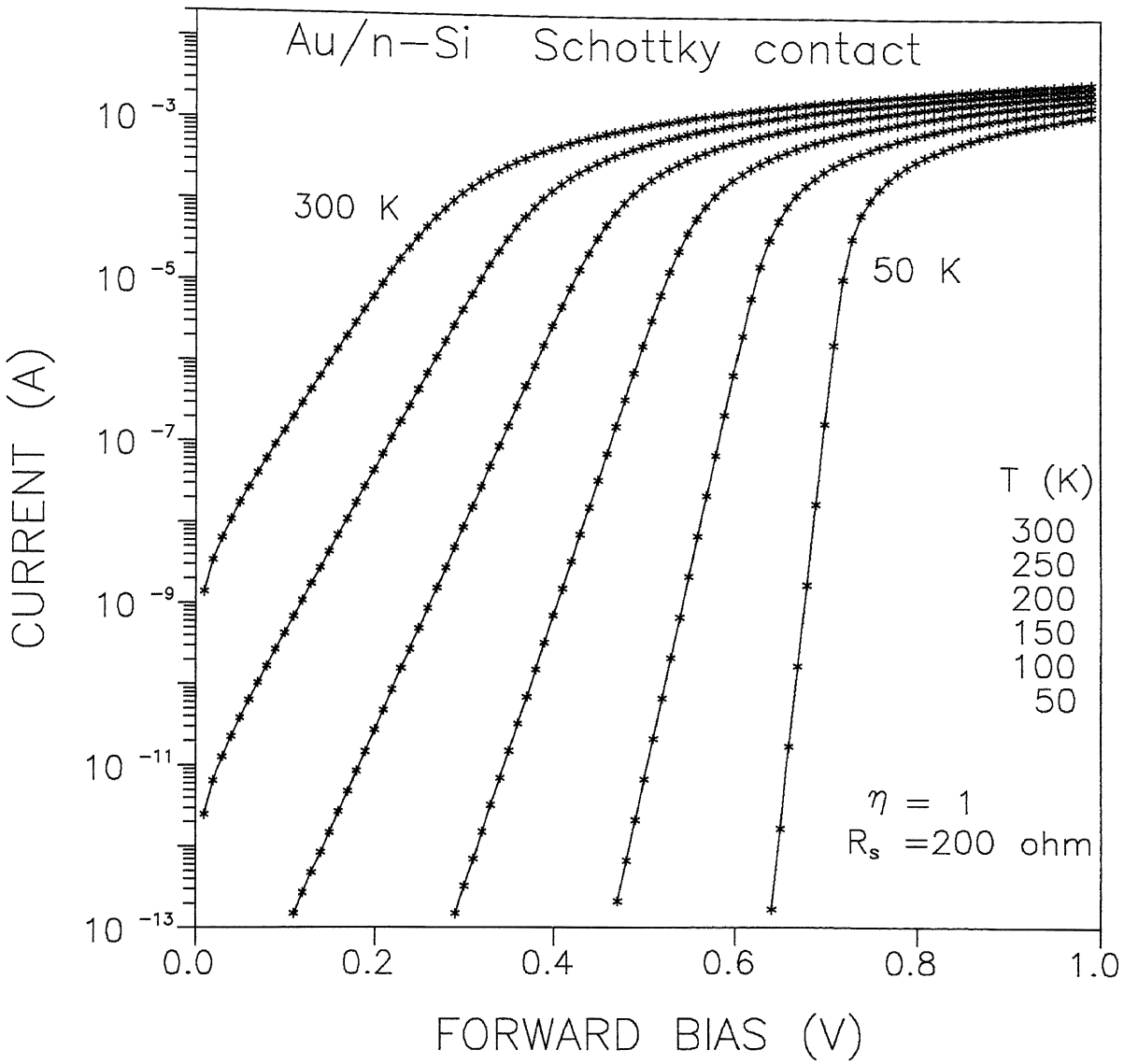


Fig. 4.8 Simulated Current-Voltage characteristics displaying effect of temperature assuming ideality factor η and series resitance R_s to be unity and 200 Ω, respectively.

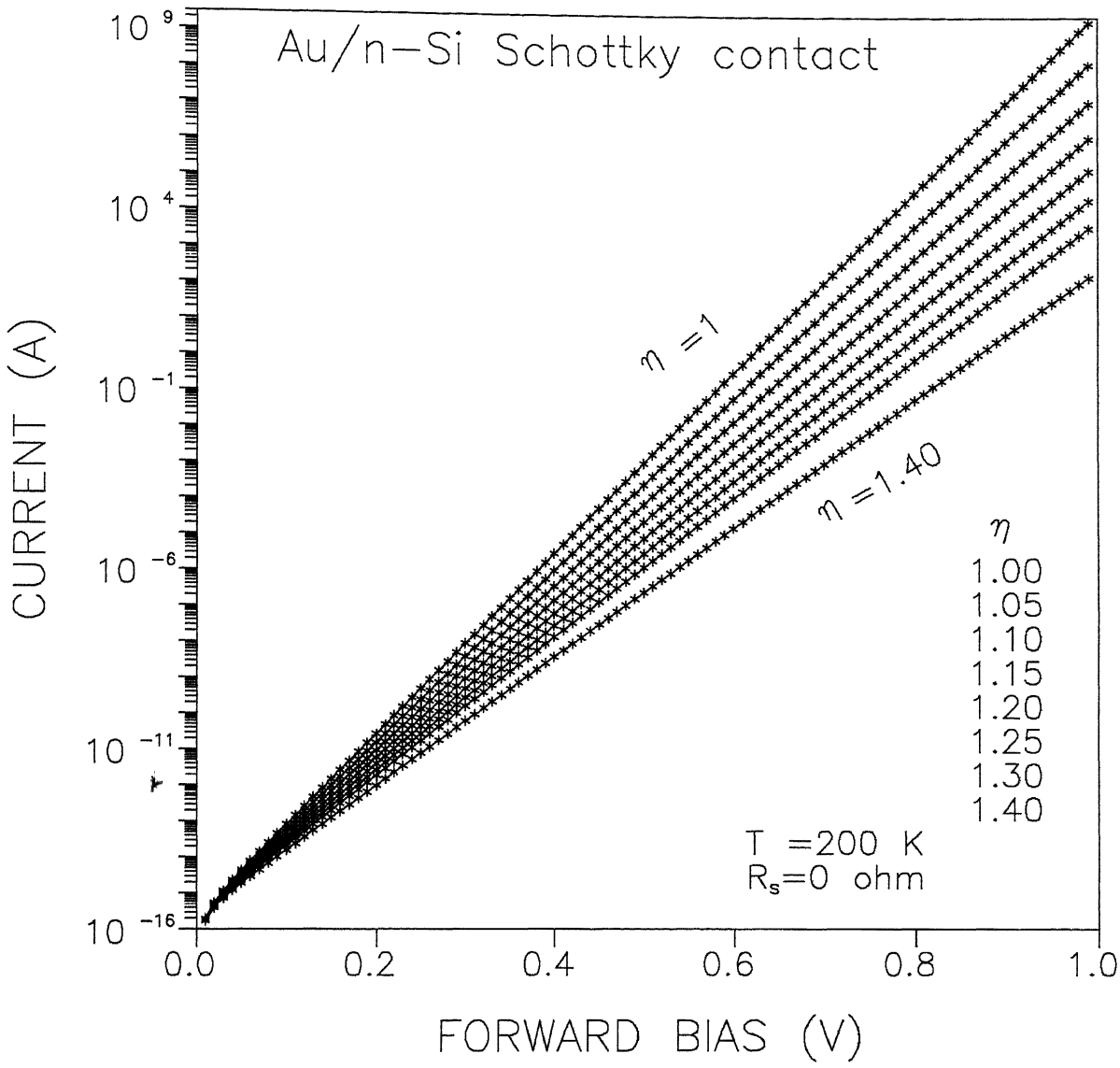


Fig. 4 9 Simulated Current-Voltage characteristics showing effect of ideality factor (η) at 200 K assuming series resistance R_s to be zero

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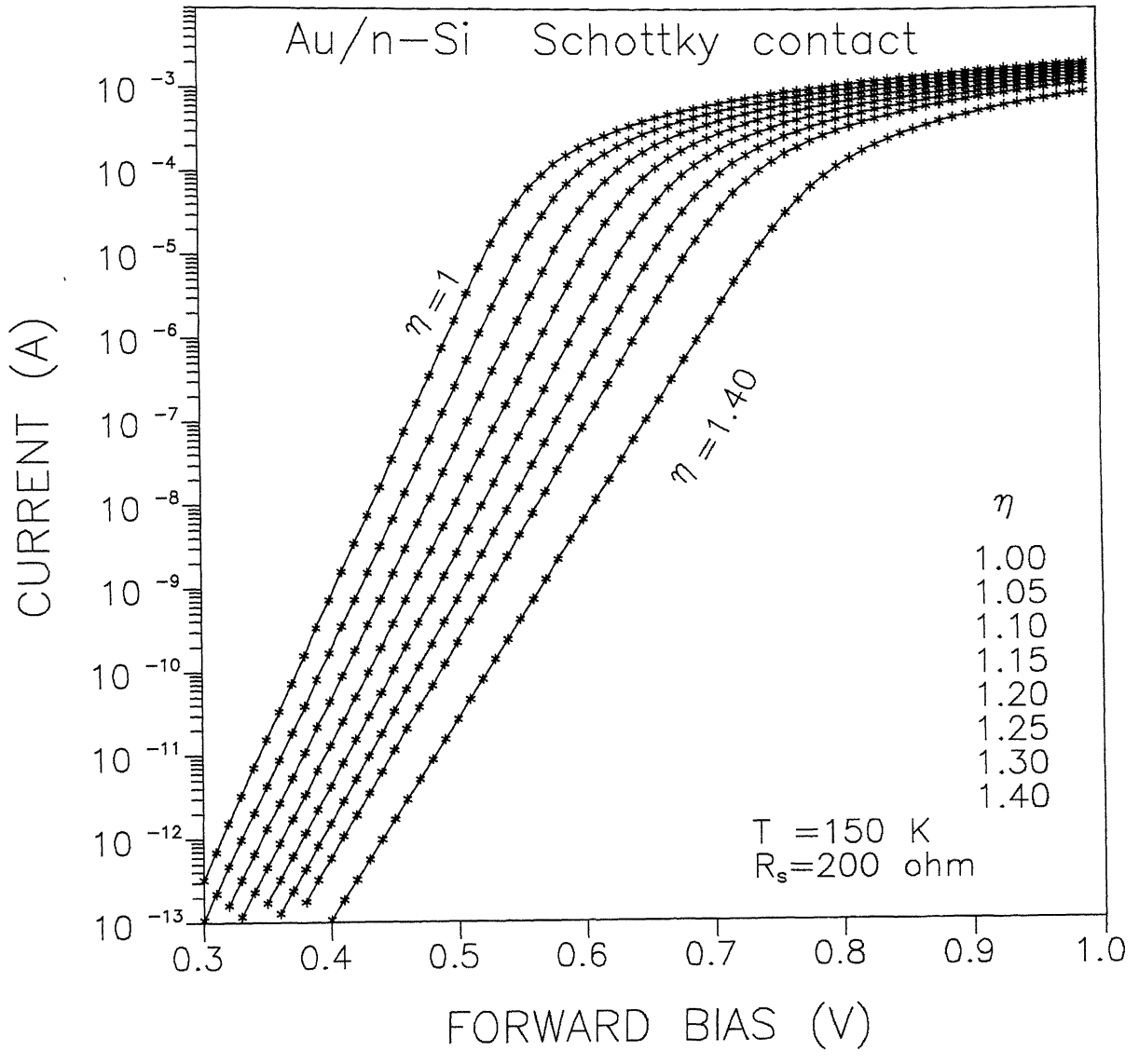
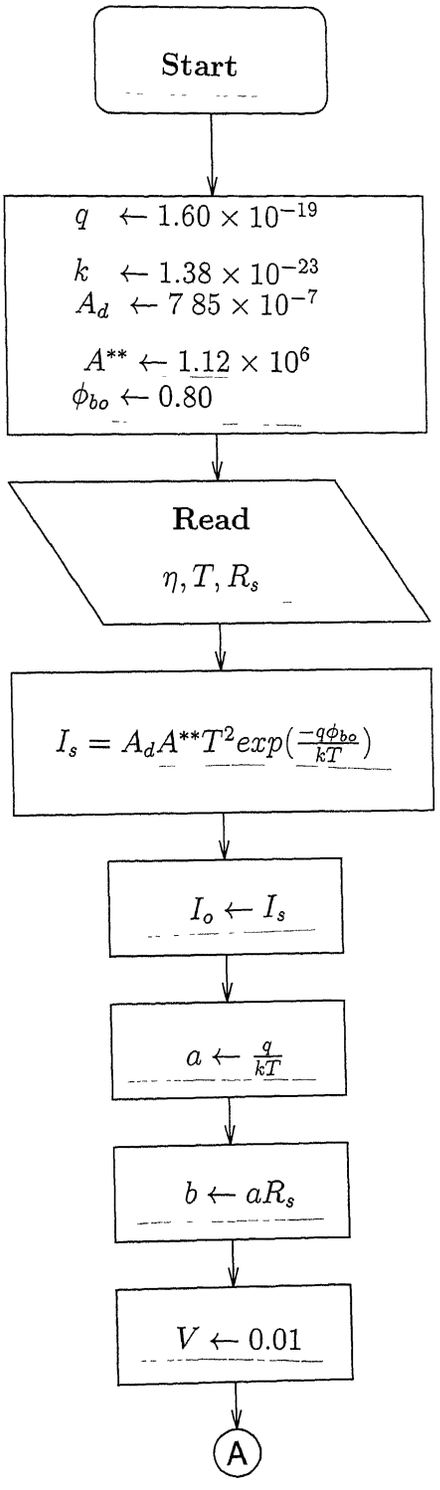
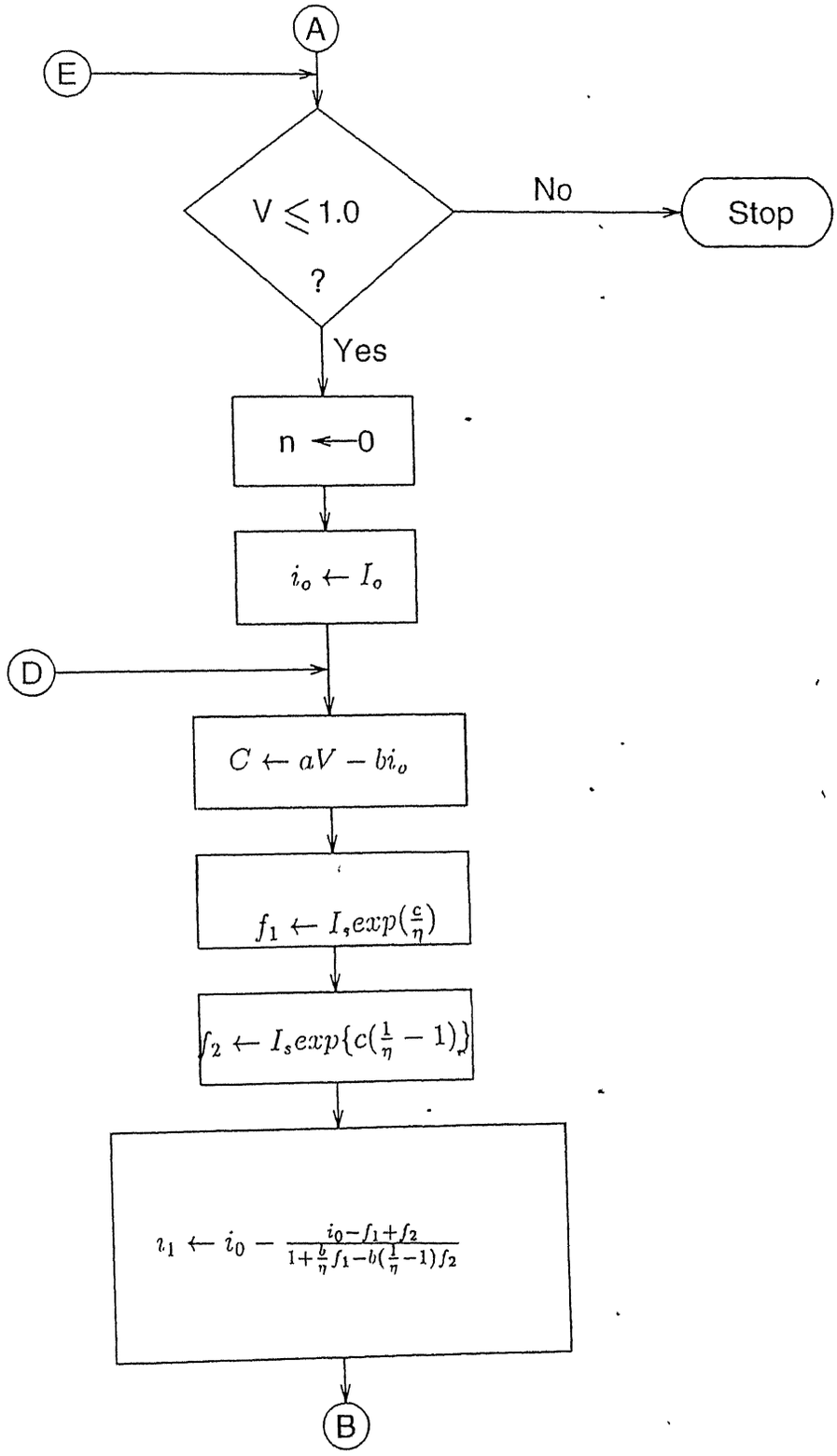
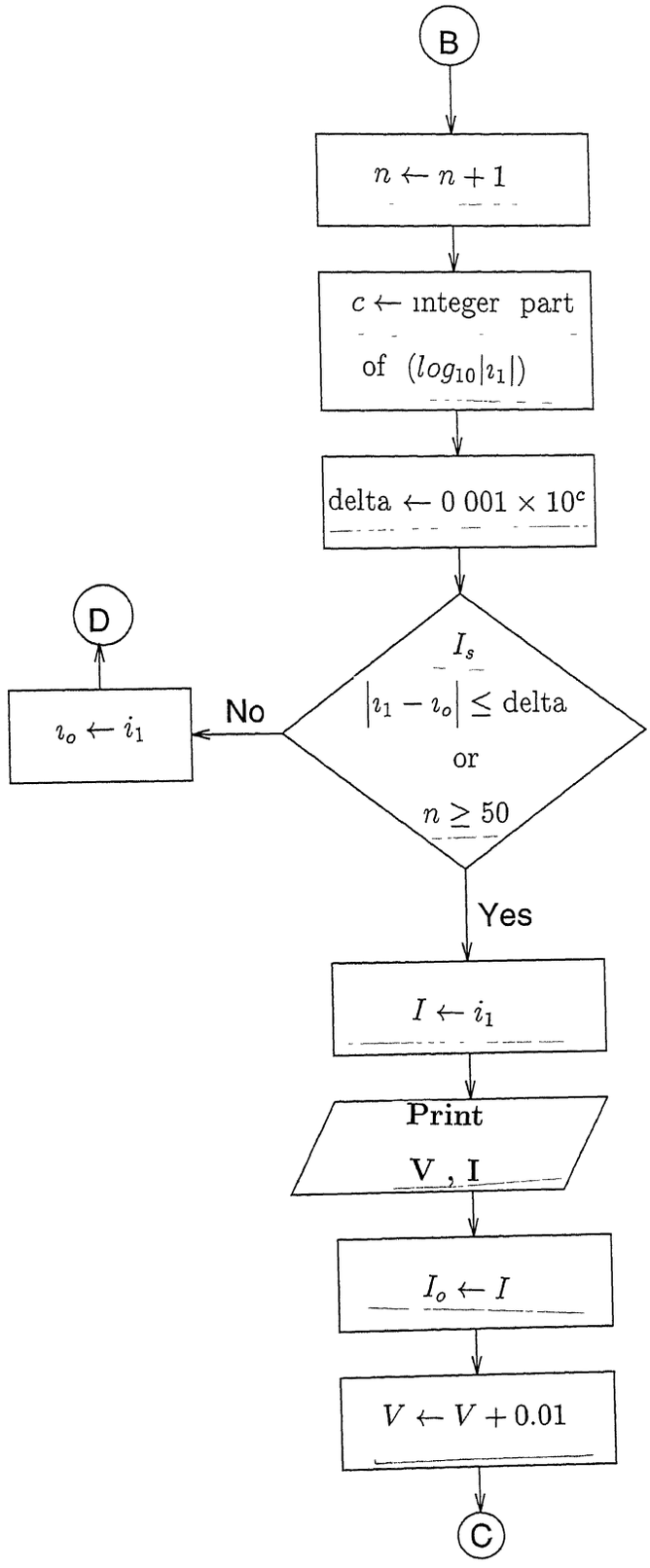


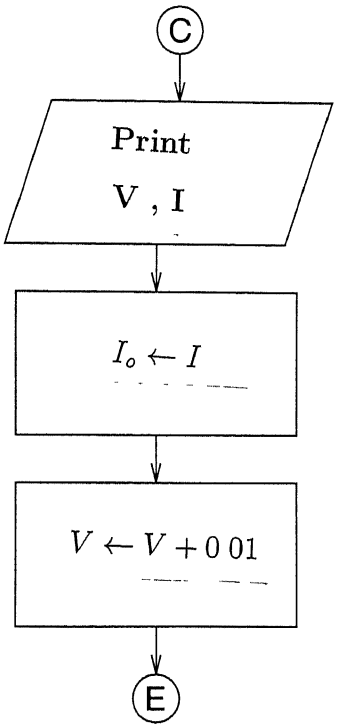
Fig. 4.10 Simulated Current-Voltage characteristics showing combined effect of ideality factor (η) and series resistance at 150 K assuming series resistance to be 200Ω .

4.3 Algorithm of simulation




A
E
V ⩽ 1.0
?
No
Stop
Yes
n ← 0
$i_o \leftarrow I_o$
D
$C \leftarrow aV - bi_o$
$f_1 \leftarrow I_s exp(\frac{c}{\eta})$
$f_2 \leftarrow I_s exp\{c(\frac{1}{\eta} - 1)\}$
$i_1 \leftarrow i_0 - \frac{i_0 - f_1 + f_2}{1 + \frac{b}{\eta} f_1 - b(\frac{1}{\eta} - 1) f_2}$
B


B
$n \leftarrow n+1$
$c \leftarrow$ integer part of $(log_{10}|i_1|)$
delta $\leftarrow 0\ 001 \times 10^c$
I_s
$|i_1 - i_o| \leq$ delta
or
$n \geq 50$
No
$i_o \leftarrow i_1$
D
Yes
$I \leftarrow i_1$
Print
V , I
$I_o \leftarrow I$
$V \leftarrow V + 0.01$
C


C
Print
V , I
$I_o \leftarrow I$
$V \leftarrow V + 0\,01$
E

4.4 Computer program in C

```
# include < stdio.h >

# include< math.h >

# define maxit 50

double I_s, I_o, delta, v, a, b, f1, f2 , /* global variable */

float η ;

main ()

{

double reduce () ;

double I, q, k, A_d, A** ;

float T, R_s, φ_bo ;

extern double I_s, I_o, delta, V, a, b ;

extern float η ;

q = 1.60e − 019 ;

k = 1.38e − 023 ;

A_d = 7.85e − 07 ;

A_** = 1.12e + 06 ;

φ_bo = 0.8 ;

scanf ("%f",& η ) ;

printf ("\n  η = %f", η) ;

scanf ("%f", & T);

printf ("\nT = %f", T) ;

scanf("%f", &Rs) ;

printf ("\nRs = %f", Rs) ;
```

$I_o = I_s = A_d * A^{**} * T^2 exp(-q * \phi_{bo}/(k * T))$;

printf ("\n$I_s$ = %le", I_s) ,

a = q/(k*T);

$b = a * R_s$;

for (V = 0 01; V ¡= 1.0; V += 0.01) {

I = reduce () ;

printf ("\n %4.2f %le" , V , I) ;

$I_o = I$;

}

}

double reduce ( ) {

void func (double i) ;

int flag = 1, n = 0 ;

double $i_o = I_o$, i1 , c ;

extern double delta, b, f1, f2;

extern float η ;

while (flag) {

func (i_o) ;

$i_1 = i_o - (i_o - f1 + f2)/(1 + b * f1/\eta - b * f2 * (1/\eta - 1))$,

++n ;

c = floor (log10 (fabs (i1))) ;

delta = .001 * pow(10, c) ;

if ((fabs(i1-i0)<= delta)|| (n >= maxit)) {

flag = 0 ;

```
return(i1);
}
else
i0 = i1;
}
}
    void func(double i)
{
extern double Is, a, b, f1, f2;
extern float η ;
double c;
    c = (a*v - b*i);
f1 = Is * exp(c/η);
f2 = Is * exp(c * (1/  eta - 1) )  ;
return    ;
}
```

Note: η *appears in place of* η_{ap} *in the above program.*

Chapter 5

Conclusion

1. Au/n-Si (111) Schottky barrier diodes can be prepared successfully by depositing a gold layer $\approx 600\mathring{A}$ thickness, using a thermal evaporation technique in vacuum $\approx 10^{-6}$ torr, onto a thoroughly cleaned n-type silicon wafer substrate.

2. I-V characteristics of the Au/n-Si (111) Schottky diodes can be explained on the basis of a thermionic emission-diffusion (TED) mechanism. The ln(I)-V plots at 300 K exhibits linearity over a wide current range but deviates beyond 0.3 V and saturates due to the effectiveness of voltage drop occuring across the series resistance R_s of the diode.

3. Several diode parameters viz., barrier height, ideality factor, series resistance and saturation current can be determined by fitting the I-V data in the TED current expression using a computer program. While the values of zero-bias barrier height lie between 0.72 and 0.79 V, the ideality factor varies from 1.16 to 1.66. The high values of the ideality factor can be attributed to the prevailing barrier inhomogeneities at the gold-silicon interface The devices can be classified into two groups depending on the values of their series resistance (R_s) i.e., R_s in the range of 213-292 Ω or in excess of 3000 Ω .

4. The values of barrier height obtained from the C-V characteristics are found to be invariably

higher than those derived from I-V characteristics This discrepancy is possibly arising due to inhomogeneities present at the metal-semiconductor junction.

5. X-ray diffraction, SEM and RBS studies reveal that gold does not react with silicon even during annealing of the Au/n-Si(111) Schottky diodes at $450°C$ for 30 min but diffuses into the semiconductor and form globules.

6. A computer program involving Neuton-Raphson iteration method can simulate I-V characteristics of a Schottky barrier diode using thermionic emission-diffusion (TED) current expression and assuming a Gaussian distribution of barrier height for the inhomogeneities present at the interface. The results suggest that the abnormal decrease of zero-bias barrier height (ϕ_{ap}), increase of ideality factor (η_{ap}) and non-linearity in the activation energy plot of the saturation current with decrease in temperature are caused by the inhomogeneities present at the metal-semiconductor interface. Also, the increasing value of the ideality factor (η_{ap}) decreases the slope of the straight line portion of lnI vs V plot The effect of series resistance is to show saturation in the I-V characteristics at higher bias.

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